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✓ **Interim Technical Report  
Semiconductor-Insulator Structures  
for the 1- to 2- $\mu$ m Region**

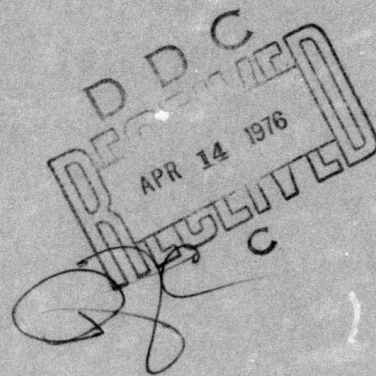
R.T. Bate, J.M. Caywood, C.R. Hewes, K.L. Lawley,  
A.R. Reinberg and W.C. Rhines

22 February 1974

Report 08-74-09 ✓

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⑥ Interim Technical Report • •  
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⑩ R.T. Bate, J.M. Caywood, C.R. Hewes, K.L. Lawley  
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## TABLE OF CONTENTS

Section	Title	Page
I	INTRODUCTION . . . . .	1-1
II	SEMICONDUCTOR PREPARATION (GaInAs) . . . . .	2-1
III	INSULATOR PREPARATION AND CHARACTERIZATION . . . . .	3-1
	A. Introduction . . . . .	3-1
	B. Insulator Characterization . . . . .	3-1
	C. Reactive Plasma Deposition . . . . .	3-2
	1. Silicon Nitride . . . . .	3-2
	2. Aluminum Oxide . . . . .	3-5
	D. Liquid Phase Anodization . . . . .	3-8
	E. Plasma Anodization . . . . .	3-11
IV	ELECTRICAL MEASUREMENTS . . . . .	4-1
	A. General Principles . . . . .	4-1
	B. Test Facilities . . . . .	4-2
	C. Surface State Measurements . . . . .	4-4
	1. Analysis of Surface State Densities in Silicon . . . . .	4-4
	2. Fast Interface State Measurements in Ge-AlO <sub>x</sub> -Al . . . . .	4-6
	3. Insulator Electrical Instabilities . . . . .	4-7
V	CONCLUSIONS . . . . .	5-1

## LIST OF ILLUSTRATIONS

Figure	Title	Page
2-1	Schematic Drawing of Ga/In/HCl/AsH <sub>3</sub> /H <sub>2</sub> Epitaxial Reactor . . . . .	2-2
2-2	Dependence of Solid Solution Composition on Input Pressures . . . . .	2-2
2-3	Surface of Ga <sub>0.65</sub> In <sub>0.35</sub> As Epitaxial Film . . . . .	2-2
2-4	Cleaved, Etched Cross-Section of Graded (Ga,In)As Epitaxial Film (InAs ≈ 35%) . . . . .	2-4
2-5	Variation of InAs Content in Epitaxial Film . . . . .	2-5
2-6	Surface Variation of InAs Content in Epitaxial Film . . . . .	2-5
3-1	Emitter Structure . . . . .	3-2
3-2	Tube Reactor With Square Insert Tube and Gas Block . . . . .	3-3
3-3	Density of Si <sub>3</sub> N <sub>4</sub> Plasma-Deposited Films as a Function of Deposition Temperature . . . . .	3-4
3-4	Histogram of Pinhole Densities in AlO <sub>x</sub> . . . . .	3-8
3-5	Anodization Apparatus Wired for Constant Current Operation . . . . .	3-10
3-6	Planar Process Development . . . . .	3-11
3-7	Diagram of Plasma Anodization Apparatus . . . . .	3-12
4-1	Block Diagram of the Instrumentation of the Test Station . . . . .	4-3

4.2	C-V and G-V Characteristics of RF Plasma Anodized Germanium . . . . .	4-5
4.3	Equivalent Circuit for MIS Capacitor . . . . .	4-6
4.4	Typical C-V and G-V Characteristics of Al-SiO <sub>2</sub> -Si at 4.0 kHz . . . . .	4-6
4.5	Surface State Conductance Versus Frequency . . . . .	4-7

## LIST OF TABLES

<i>Table</i>	<i>Title</i>	<i>Page</i>
2-1	Growth Parameters for (Ga,In)As Graded Alloys . . . . .	2-4
3-1	Gas Composition to Obtain Refractive Index of 2.0 . . . . .	3-4
3-2	Neutron Activation Analysis Impurity Concentrations . . . . .	3-6
3-3	Surface Preparation Procedure . . . . .	3-7
3-4	Stoichiometric Ratios of the Deposited Layer Calculated From Backscattering Analysis . . . . .	3-8

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## SECTION I INTRODUCTION

The goal of this contract is to develop, fabricate, evaluate, and deliver to NVL thin-film structures consisting of semiconductors having bandgaps on the order of 0.7 eV and compatible insulators. The following requirements are also goals:

- High-field tunneling transport,
- Semiconductor surface passivation,
- Semiconductor masking for diffusion and selective etching,
- Surface charge transport,
- Antireflection coatings.

Activities of the program include semiconductor material preparation (GaInAs), insulator preparation, and characterization by both electrical and nonelectrical techniques of semiconductor-insulator structures.

The primary semiconductor vehicles for this study have been GaSb and GaInAs, but early work was done on germanium; silicon was used as a control substrate for insulator depositions throughout the program. Present plans are to concentrate for the remainder of the program on  $\text{Ga}_{0.5}\text{In}_{0.5}\text{As}$ , which has a 0.7-eV band-gap, and to continue to use silicon and germanium as a control substrate.

The emphasis in insulator preparation has been on low-temperature processing to prevent degradation of semiconductor properties. Three techniques are being explored: reactive plasma deposition (RPD) which is being used to deposit  $\text{AlO}_x$ ,  $\text{SiO}_x$ , and  $\text{SiN}_x$ ; liquid-phase anodization for native oxides and sulfides; and plasma anodization also for native insulators.

## SECTION II

### SEMICONDUCTOR PREPARATION (GaInAs)

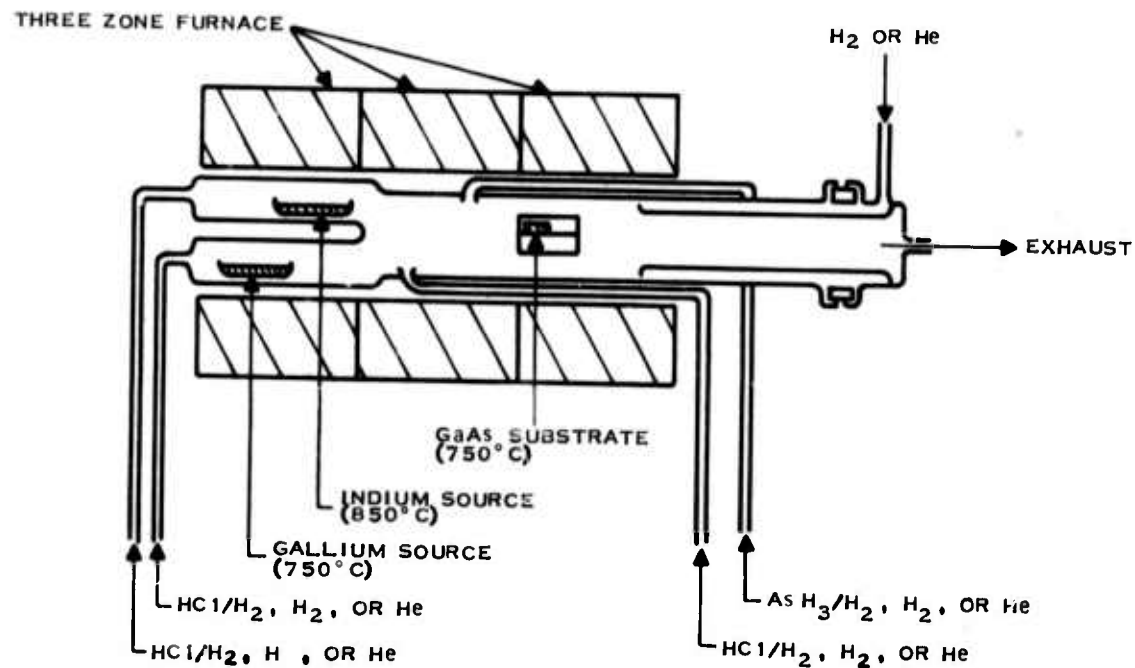
As part of the investigation of semiconductor-insulator structures for the detection of radiation in the range of 1 to 2  $\mu\text{m}$ , solid-solution alloys of GaAs and InAs were chosen because of the monotonic variation from about 0.9 to 3.48  $\mu\text{m}$  of the bandgap of this alloy system. Alloys of the composition  $\text{Ga}_{0.5}\text{In}_{0.5}\text{As}$  with a bandgap of  $\sim 1.7 \mu\text{m}$  have been specifically chosen for this investigation.

The materials program has centered about preparing this alloy composition by the different techniques of vapor phase epitaxy. The first of these is synthesis of the alloys using an alloy of gallium dissolved in indium as the source for the Group III elements. This system was used because it was in operation at the beginning of the program. Modification of the system for the growth of 50 percent alloy, both p- and n-type, was carried out and reported in the first Semiannual Report<sup>(1)</sup> on this contract. This reactor system is still being used for the preparation of test materials. Its major disadvantage, however, is that graded epitaxial films cannot be made in it.

It was recognized at the start that compositional grading would be essential for the improvement of structural and electrical properties of the alloys. Compositional grading allows for reduced strain arising from the lattice mismatch between the GaAs substrate and the epitaxial alloy film grown upon it. For this reason, a dual-source reactor, separate gallium and indium reservoirs with separate HCl supplies, was designed and put into operation. Progress in the growth of  $\sim 50$  percent (Ga,In)As is discussed in the remainder of this section.

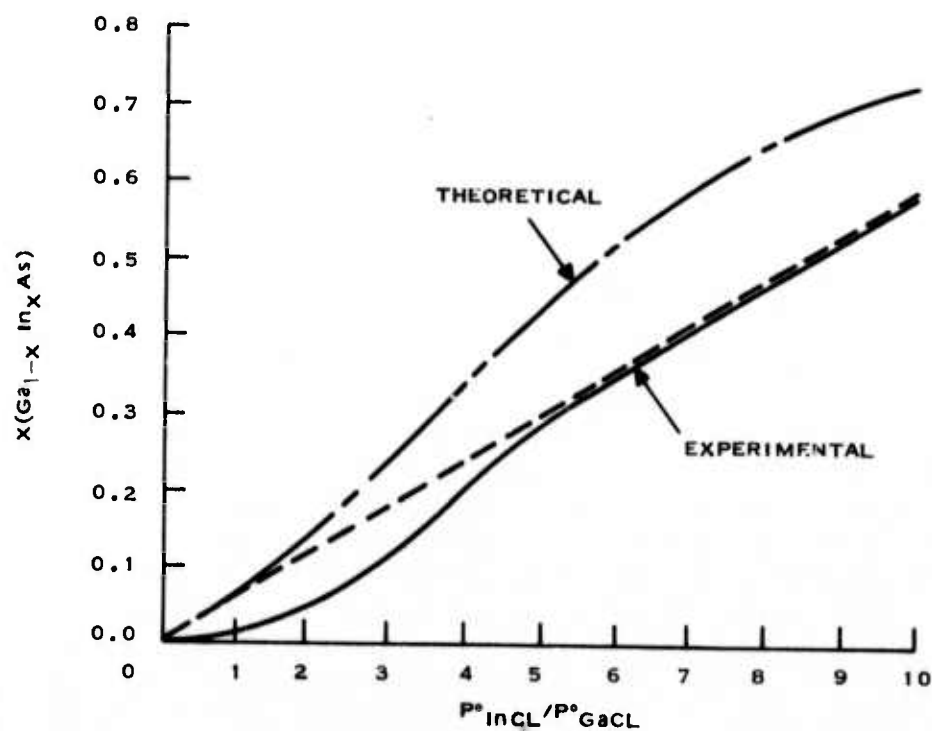
The dual-source reactor constructed for use on this program is shown schematically in Figure 2-1. The chemistry of the  $\text{HCl-AsH}_3$  system has been described in the literature<sup>(2,3)</sup>. Two important differences have been incorporated into this reactor: a separate source of HCl gas to prevent predeposition on the walls of the reactor in the region where the reagents mix, and an exhaust system to prevent deposition in the cold section of the tube. This latter feature allows for cleaning of the reactor *in situ* with HCl gas at high temperatures and minimizes contamination which might occur during disassembling and acid cleaning.

The preparation of (Ga,In)As alloys is complicated by the fact that the standard free energies of GaAs and InAs differ by about 4 Kcal/mole at 750°C, with GaAs being higher. For this reason, the deposition of GaAs is favored. To prepare a 50 percent alloy, ratios of In to Ga in the gas phase must be 8.5 to 1. A graph showing the experimental results for various gas composition is shown in Figure 2-2. Data from this graph were extracted from the literature<sup>(2,3)</sup>. The results of the present work correspond to the upper curve in the range of 5 to 50 percent InAs alloys. Theoretical predictions of the relationship between gaseous and alloy composition differ appreciably from experiment as shown in Figure 2-2. At an input ratio of 8.5, a theoretical composition of about 68 percent should be observed instead of the 50 percent InAs actually observed. This departure from theoretical has not been investigated; however, growth under these conditions is probably a kinetically limited process. In this case, departures from theoretical are not surprising.



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Figure 2-1. Schematic Drawing of Ga/In/HCl/AsH<sub>3</sub>/H<sub>2</sub> Epitaxial Reactor



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Figure 2-2. Dependence of Solid Solution Composition on Input Pressures

The outstanding problem in preparing alloys is compositional uniformity. A  $\pm 2$  percent variation in the input ratio at 8.5 would result in a variation in composition from about 48 to 52 percent InAs in the solid. Variations of 2 percent are not uncommon, owing to instability of flow control, transient reaction conditions, and poor mixing of the gaseous reactants.

The preceding discussion shows some of the problems and considerations associated with preparing good (Ga,In)As alloys. The results of the first experiments in preparing graded alloys and the direction of future work based upon these considerations conclude this section.

Initial attempts at preparing abrupt heteroepitaxy similar to that grown in the alloy source reactor were unsuccessful for compositions with InAs above 15 to 20 percent. The exact cause of this difference is not understood. A sample from the alloy reactor was checked for variations in In content from the substrate to air interfaces with the electron microprobe. No natural grading owing to differences in reactivity of the In and Ga sources was observed. The samples prepared in the dual-source system were granular with no apparent single crystal regions. If the difference is not caused by grading, microscopic variations in composition of the depositing material could account for the inferior structure. That better homogeneity would be expected from the alloy source may account for the difference. This problem remains unsolved but has not hampered continuation of the growth of high InAs content alloys.

To establish approximate growth conditions for growing graded alloy structures, manual adjustment of the input gases was used. This procedure does not allow for continuous grading but has been successful in the preparation of alloy of up to 50 percent InAs. The procedure is first to grow a GaAs layer between 10 and 20  $\mu\text{m}$  thick, increase the HCl input to the In source, and decrease it to the Ga source in steps to a gas composition which corresponds to that required to grow a given alloy composition. Grading of about 2 percent InAs/ $\mu\text{m}$  has been used. A constant composition layer of alloy from 20 to 40  $\mu\text{m}$  thick is then grown over the graded layer. Growth conditions used to prepare a 35 percent InAs graded layer are given in Table 2-1. As seen in Figure 2-3, a cross-hatched pattern owing to the formation of misfit dislocations is observed on a slice repaired using these conditions. A cleaved and stained (A-B etch) cross-section of the epitaxial layers is shown in Figure 2-4. Here the steps in composition are clearly observed in the graded region. The variation of InAs content as determined by the electron microprobe is shown in Figure 2-5. Clearly, the gradation of composition is not linear with distance. This non-linearity is expected from the nonlinearity of the input flow rates. Growth rates for the various areas for this and similar runs were observed to be 15 to 20, 10 to 15, and 5 to 10  $\mu\text{m/hr}$  for the GaAs, graded region, and the constant composition alloy region,

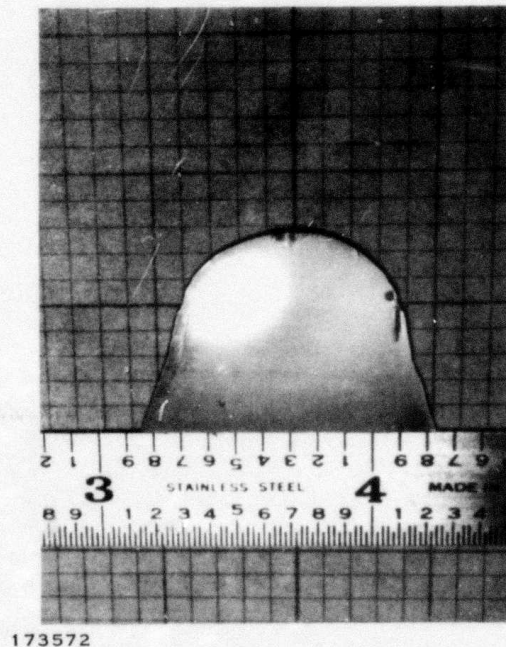


Figure 2-3. Surface of  $\text{Ga}_{0.65}\text{In}_{0.35}\text{As}$  Epitaxial Film

TABLE 2-1. GROWTH PARAMETERS FOR (Ga,In)As GRADED ALLOYS

Substrate Temperature		735°C
Ga and In Source Temperatures		850°C
AsH <sub>3</sub> (10%)/H <sub>2</sub>	90 → 245	cc/min
HCl (10%)/H <sub>2</sub> to In	0 → 165	cc/min
HCl (5%)/H <sub>2</sub> to Ga	160 → 50	cc/min
HCl (10%)/H <sub>2</sub> to Excess	25	cc/min
Final In/Ga = 6.6		Approximate Composition Ga <sub>0.65</sub> In <sub>0.35</sub> As

$$\frac{\text{In} + \text{Ga}}{\text{As}} = 0.9 \text{ to } 0.8 \text{ (Excess Arsenic)}$$

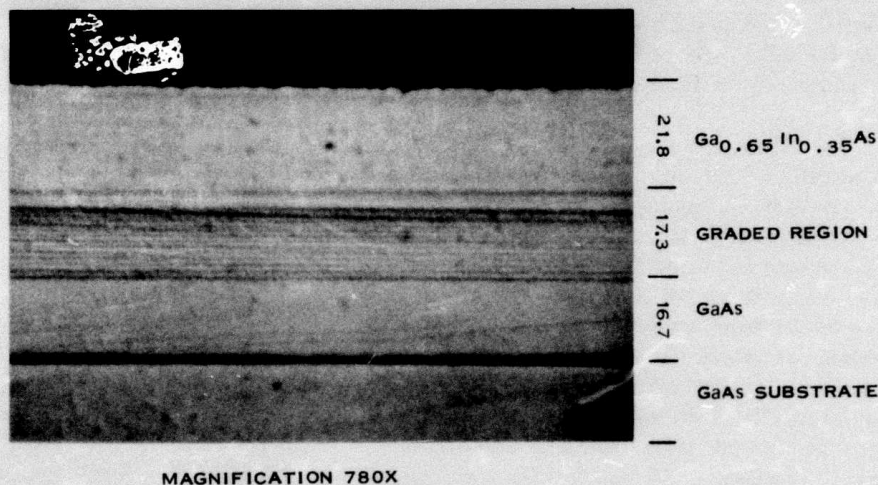
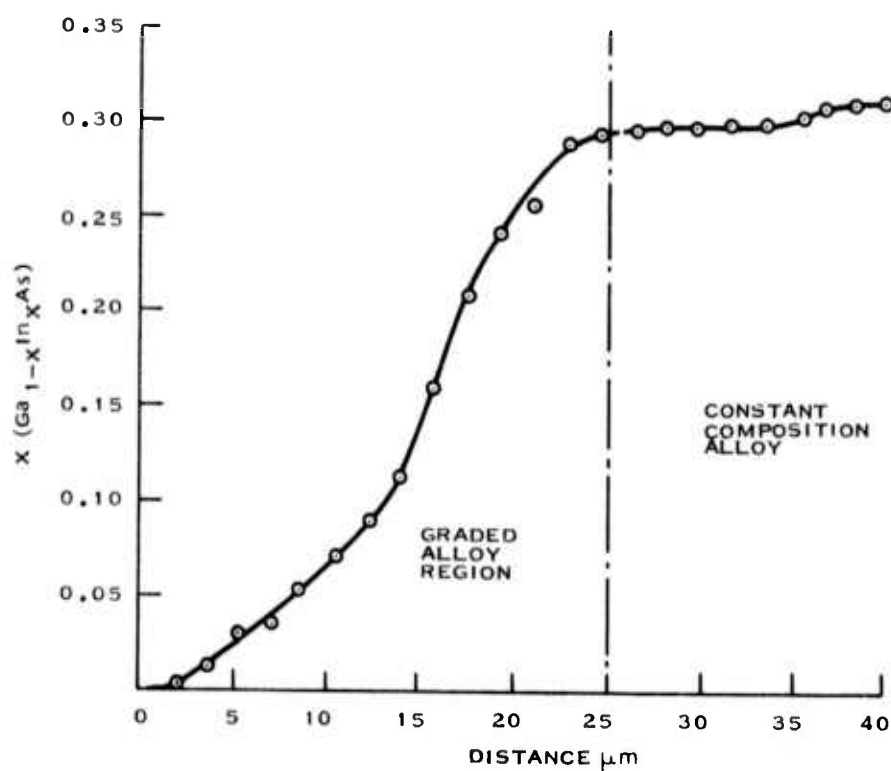


Figure 2-4. Cleaved, Etched Cross-Section of Graded (Ga,In)As Epitaxial Film (InAs ≈ 35 percent)

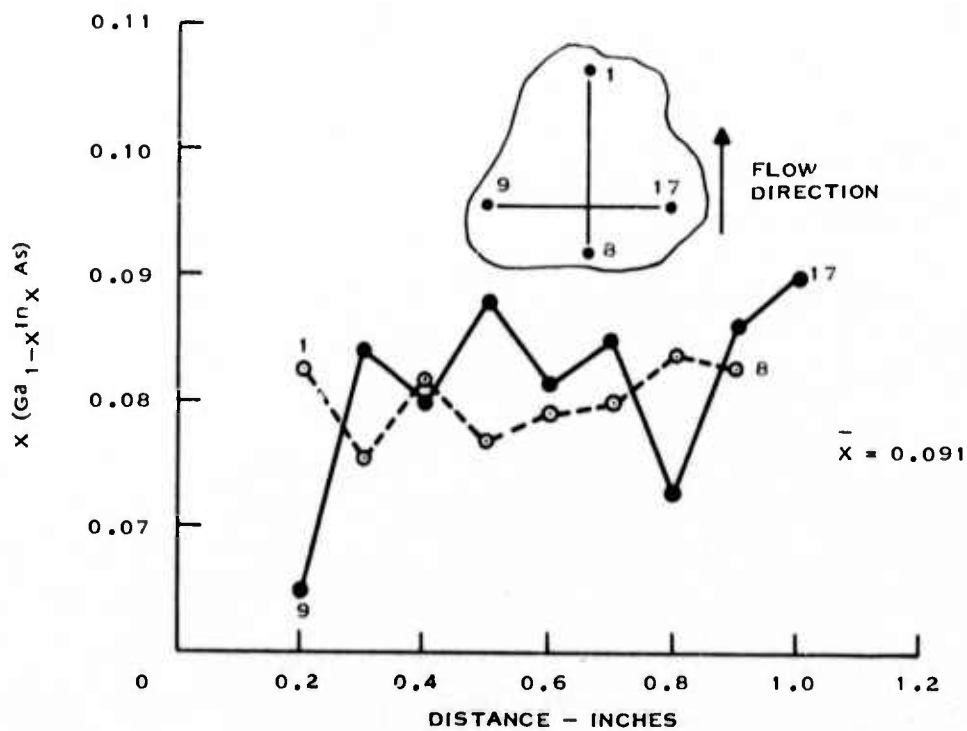
respectively. The variation of the InAs content across slice with an average composition of 9.1 percent InAs is shown in Figure 2-6. The variation across the slice is from 7.5 to 10.0 percent; however, in the flow direction, it is only 8.5 to 9.4 percent. A sample of 35 percent InAs alloy was angle lapped on a 54-degree angle and then stained with A-B to reveal etch pits associated with dislocations. A count of these pits gave a density of slightly greater than  $10^6/\text{cm}$ . As yet, no electrical evaluation of these films has been made.

From these experiments, conditions for growing graded, high InAs content alloys have been established. No optimization of grading has been carried out. In the next stage of this development, an improved grading system using reservoirs and mass flow controllers will be installed in the system. These will provide for continuous grading and for better stability and control of the input reactants. Electrical and structural evaluations of these materials will then be performed. During the intervening period, the alloy source reactor will be used for materials supply.



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Figure 2-5. Variation of InAs Content in Epitaxial Film



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Figure 2-6. Surface Variation of InAs Content in Epitaxial Film

## SECTION III

### INSULATOR PREPARATION AND CHARACTERIZATION

#### A. INTRODUCTION

Preparation of thin insulator films on semiconductors in this program was aimed at the development of low temperature growth techniques, including primarily plasma deposition, anodization in a liquid electrolyte and anodization in a gas discharge. Emphasis on low-temperature processing is important because of the interest in using compound semiconductors, such as  $\text{Ga}_x\text{In}_{1-x}\text{As}$  for the detection of  $1-2\text{ }\mu\text{m}$  radiation. The shifting lattice defect equilibrium as well as the probability of impurity contamination (particularly from Cu) associated with high-temperature processing of these materials creates substantial problems. As a result of the process development in this program, both the plasma deposition and the anodization approaches have been shown to be satisfactory growth techniques for high quality insulators with insulator semiconductor interface properties suitable for the future fabrication of devices.

Appendixes A, B, and C are listings of the samples prepared during the program using each of the three growth techniques. Because of the limited supply of  $\text{Ga}_{0.5}\text{In}_{0.5}\text{As}$ , most of the optimization of insulator properties was done using films grown on GaSb, Ge, or Si substrates. Silicon substrates were particularly useful because variations in insulator properties can be characterized without problems of extraneous variables from the substrate.

Appendix D lists samples that have been delivered to NVL for evaluation. Initially insulator-semiconductor structures were delivered with metallized dot patterns on the insulator surface to allow for electrical characterization. Later samples were delivered without these dots, at the request of NVL. Thin film "emitter structures" for application in high field tunneling experiments were also included among the deliverable items. Figure 3-1 shows the processing steps used in the fabrication of these structures.

Of the plasma-deposited insulators,  $\text{AlO}_x$  proved to be the most promising, principally because of its high breakdown strength. The  $\text{AlO}_x\text{-Ge}$  system was therefore chosen for optimization during the last half of the program. This effort led to the reproducible fabrication of nearly pinhole-free  $\text{AlO}_x\text{-Ge}$  structures which exhibited surface state densities in the  $3-5 \times 10^{11}\text{ cm}^{-2}\text{ eV}^{-1}$  range.

Of the anodic insulators, those produced by anodization in a plasma provided the most promising results, and optimization centered on oxidation and nitridation of Ge and  $\text{Ga}_x\text{In}_{1-x}\text{As}$ . Insulators produced by this technique have few or no pinholes and, in the case of  $\text{GeO}_x$ , show reasonably stable electrical properties with surface state densities again in the  $3-5 \times 10^{11}\text{ cm}^{-2}\text{ eV}^{-1}$  range.

#### B. INSULATOR CHARACTERIZATION

Development and optimization of insulator-semiconductor systems for the program required a complete nonelectrical characterization effort. This portion of the program included characterization of physical, chemical, and structural properties of most types of insulators, on a continuing basis, to evaluate modifications to the growth techniques.

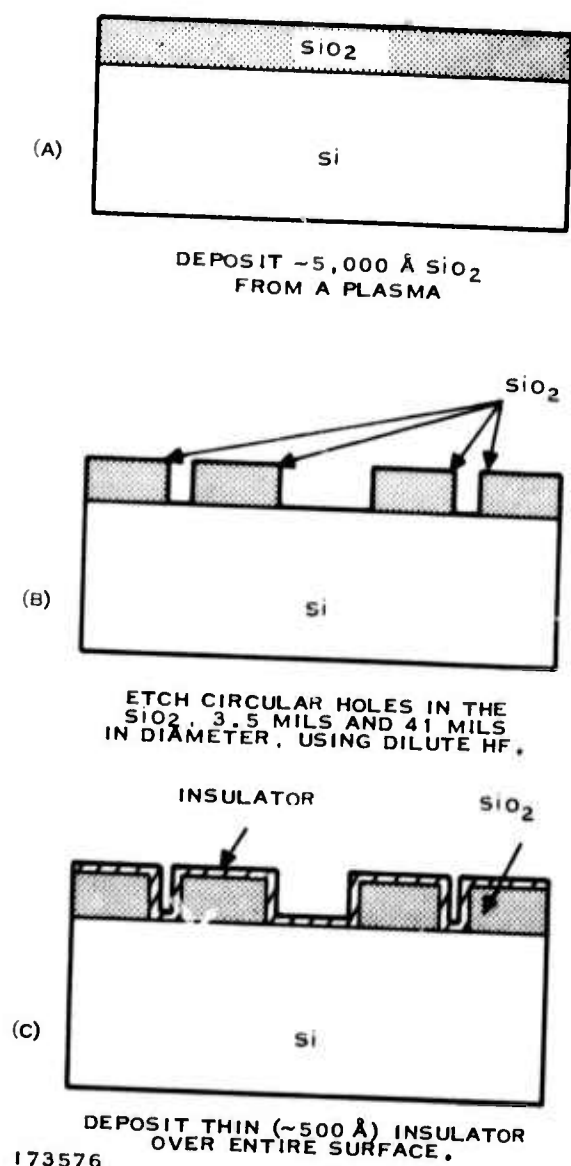


Figure 3-1. Emitter Structure

Physical properties which have been examined for the insulators include thickness, index of refraction, pinhole densities, surface morphology, and substrate cleanliness. Ellipsometry (or talysteping), optical microscopy, scanning electron microscopy, and electrophoretic pinhole detection have been used routinely to measure these properties. The chemical composition measurements were made to determine bulk constituents in the insulators, stoichiometric variations, and trace impurity content. Techniques used included ion-backscattering, Auger analysis, X-ray diffraction, and neutron activation analysis. Structural characteristics were examined primarily to determine the type of bonding in the amorphous insulators and to detect crystallinity. Infrared absorption spectra have been analyzed for the bonding studies, and prolonged X-ray exposure of insulators in a Debye-Scherrer camera has been used to look for crystallinity.

### C. REACTIVE PLASMA DEPOSITION

#### 1. Silicon Nitride

Reactive plasma deposition is a chemical vapor deposition (CVD) method of producing thin films of dielectric insulators. It differs from ordinary CVD in that all or part of the energy necessary to initiate the reaction is provided by the collisional excitation obtained in a low-pressure discharge of the reactant gases. Although plasma polymerization of organic compounds<sup>4</sup> is a well-known process with a long history, the process for depositing inorganic films, particularly silicon-nitrogen compounds, was first reported in 1965 by Sterling and Swann.<sup>5</sup>

Organosilicon films formed by an RF plasma polymerization process<sup>6</sup> have been found to be useful as dielectric waveguides for integrated optical devices. Interest in the inorganic films, however, has been concerned primarily with their possible uses as insulators for various types of electronic and semiconductor devices. Most significant to this application is the fact that films may be deposited at low temperatures, precluding the need for special constraints on substrate conditions. Thus, it is possible to deposit high-quality dielectric films on materials that cannot, for one reason or another, be subjected to high temperatures. In addition, the RPD method provides a degree of flexibility in material selection not available from other low-temperature processes such as sputtering.

A simple form of reactor for the deposition of thin films, either by ordinary CVD or by RPD, consists of a horizontal tube through which the gases are allowed to flow. For some types of reactions, it is possible to stack material, such as silicon slices, so that they fit into the tube with their faces perpendicular to the tube axis. It is much more common in CVD reactors, however, to have material lie flat with the face to be coated parallel to the direction of the tube axis, which is also the direction of gas flow. This geometry also provides a simple means of obtaining uniform RF-excited glow discharges and is shown in Figure 3-2. Apparatus similar to this has been used to deposit a variety of films. The three most widely investigated materials are silicon nitride, silicon oxide, and aluminum oxide.

Silicon nitride (or, more properly, polysilazane) as deposited by RF plasma techniques is a glassy, completely amorphous material the properties of which depend on the composition of the reactant gases and the temperature of deposition. An excellent description of the nature of these glassy silicon-based compounds has been given by Phillip.<sup>7,8</sup> Basically the structure of these materials is believed to consist of Si tetrahedra of the type  $\text{Si}(\text{Si}_x\text{O}_y\text{N}_z)$  with x, y, and z determined in a statistical manner from the concentrations of the respective species in the gas phase.

The silicon nitrides used in this study have been grown from gas mixtures containing  $\text{SiH}_4:\text{N}_2:\text{NH}_3:\text{Argon}$  in various ratios. The particular ratio depends on the temperature of the deposition and the desired refractive index of the film. Table 3-1 is a compilation of the gas composition used to obtain a refractive index of 2.0 at temperatures ranging from 100° to 350°C. Values given are the fraction of the total gas flow for each component.

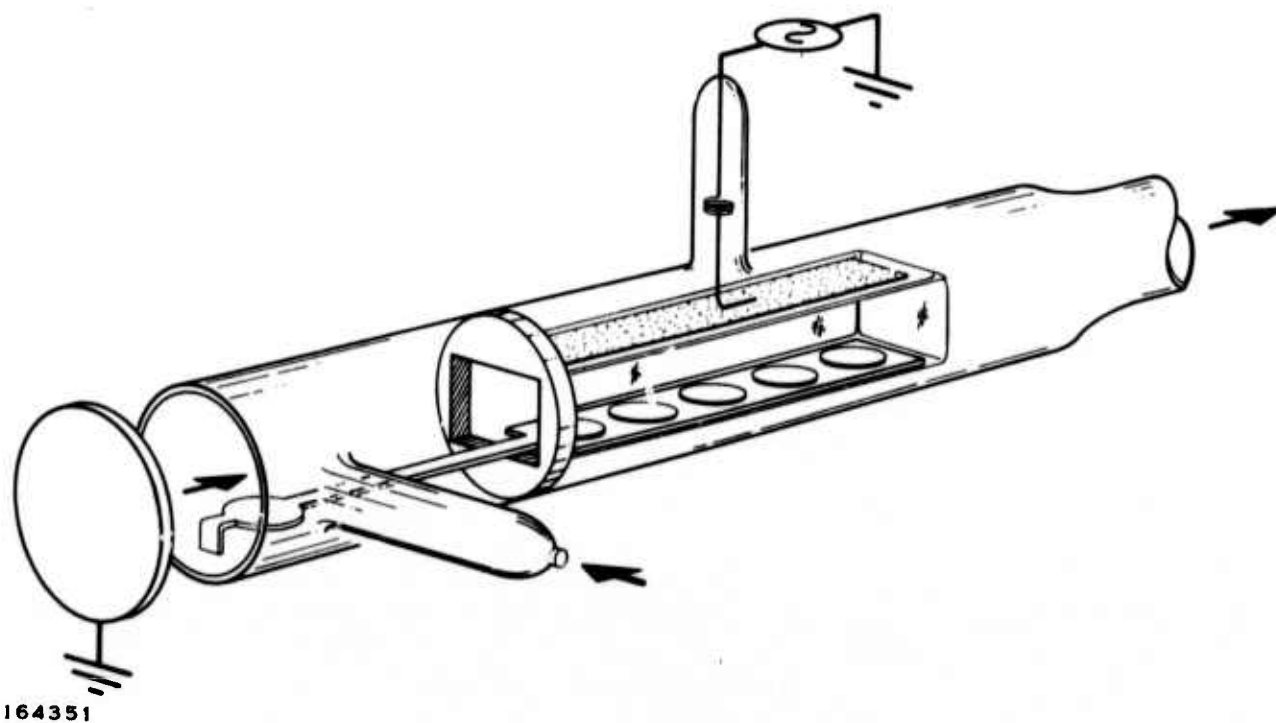


Figure 3-2. Tube Reactor With Square Insert Tube and Gas Block

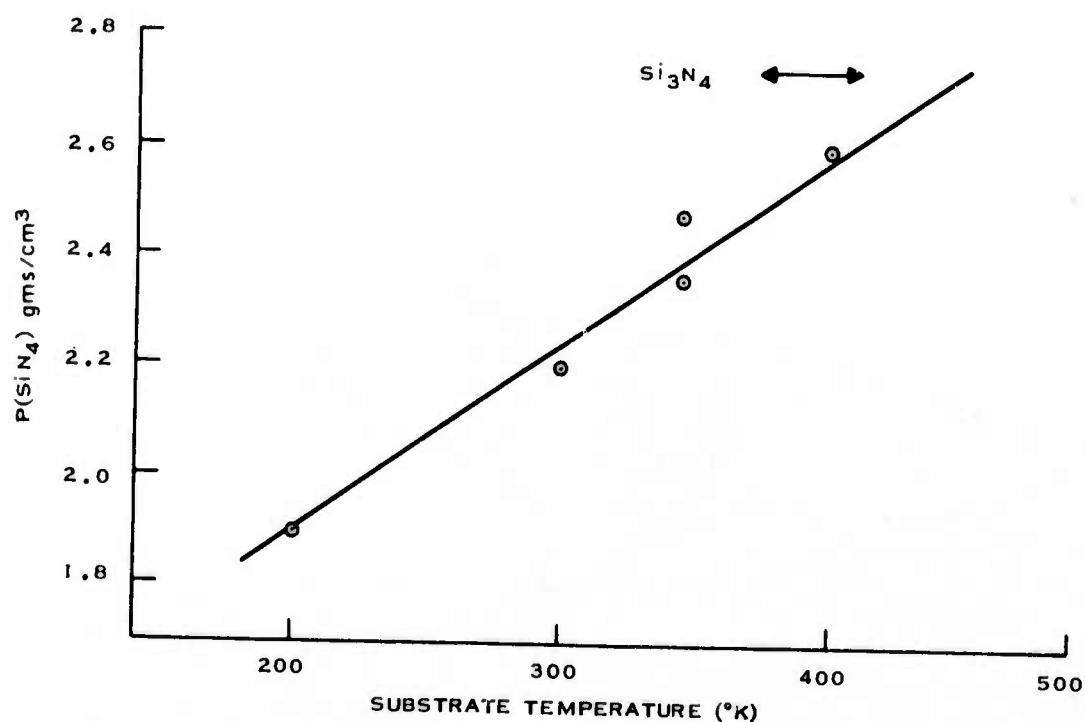
TABLE 3-1. GAS COMPOSITION TO OBTAIN REFRACTIVE INDEX OF 2.0

Temperature (°C)	SiH <sub>4</sub>	N <sub>2</sub>	NH <sub>3</sub>	Ar
100	0.021	0.483	0.011	0.485
250	0.019	0.454	0.016	0.510
300	0.018	0.427	0.021	0.534
350	0.017	0.401	0.026	0.555

It is significant that the amount of ammonia needed to produce material with an index near 2.0 increases substantially as the substrate temperature used during deposition is increased from 100°C to 350°C. It may be correlated with the increase in density of the films. Figure 3-3 shows the density of the films as determined by weighing a known thickness as a function of the substrate temperature during deposition. It is well-known that the refractive index of nitrides or oxides increases as the silicon content of the film exceeds the stoichiometric concentration. The refractive index,  $n$ , also depends linearly on the density,  $\rho$ , of the films according to the relation.

$$\frac{n^2 - 1}{n^2 + 1} = \sum_i \frac{\rho_i B_i R_i}{W_i}$$

In this expression,  $R_i$  is the bond refractivity of the  $i$ th type of bond,  $B_i$  is the bond fraction, and  $W_i$  is the molecular weight. The summation is taken over all types of bonds present



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Figure 3-3. Density of Si<sub>3</sub>N<sub>4</sub> Plasma-Deposited Films as a Function of Deposition Temperature

in the material. For example, for  $\text{Si}_3\text{N}_4$ , the bond refractivity,  $R_i$ , refers only to the Si-N bond and has a value computed to be 1.93;  $B_i = 12$  and  $W_{\text{Si}_3\text{N}_4} = 140$ . The value of  $R$  for an Si-Si bond is considerably greater, being about 5.9. Thus, small excesses of silicon can substantially increase the refractive index. For films prepared at the lower temperature, the silicon content for fixed refractive index is expected to be greater than for films prepared at higher temperatures since the density is less. The density of the films prepared in this manner compares very favorably with that of those reported by Meyer and Scherber<sup>9</sup> for plasma-deposited nitrides made from silane and  $\text{N}_2$ .

Silicon oxides (polysiloxanes) have been prepared for evaluation as insulators in a manner similar to that for the nitrides but with different gases. Originally, a silane:argon-nitrous oxide:nitrogen composition was used. This system has the advantage that the structure of films is relatively insensitive to the gas composition, if the nitrous oxide concentration exceeds about 10 percent of the nitrogen concentration. An oxygen-containing gas is used (rather than pure  $\text{O}_2$ ) which does not react with silane except in the region in which the glow is established. It was observed that, when the oxygen containing gas was  $\text{N}_2\text{O}$ , there was always a small homogeneous reaction that produced a fine powdery silica product. This product was detrimental to the vacuum pumps used and is also believed to produce powdery deposits that lead to pinholes. It is not known if the homogeneous (gas phase) reaction is a true small but finite reaction rate between the silane and the  $\text{N}_2\text{O}$ , if it is caused by a thermally induced decomposition of the  $\text{N}_2\text{O}$  and subsequent reaction between the  $\text{SiH}_4$  and the resultant  $\text{O}_2$ , or if it is a result of impurities in the  $\text{N}_2\text{O}$  which can be obtained only in medical grade. Mass spectrometer measurements failed to reveal the presence of free  $\text{O}_2$  in the bottled gas; the major impurity was identified as argon. The Matheson Gas Data book, however, lists the principal impurity as being about 1.5-percent air which would explain the small homogeneous reactions observed.

To avoid the possible complications of the homogeneous reaction, the oxygen-bearing gas was switched to instrument grade  $\text{CO}_2$ , a 99.99-percent minimum purity. No homogeneous gas reaction has been observed with this system. Use of  $\text{CO}_2$  is complicated by the fact that film stoichiometry, as indicated by refractive index measurements, is much more sensitive to gas concentrations. Very high  $\text{CO}_2:\text{SiH}_4$  ratios are needed to produce films with indices near 1.46, the accepted value for silica. For these films, the ratio  $\text{SiH}_4:\text{Ar}:\text{CO}_2 = 0.008:0.146:0.846$ . It is possible with this system to produce films with widely varying amounts of silicon, going all the way from amorphous silicon to a subsilicon oxide. The structure of these films has also been discussed by Phillip.<sup>7</sup> Impurity content of both  $\text{SiO}_x$  and  $\text{SiN}_x$  films was examined by neutron activation analysis. Results are shown in Table 3-2.

Film-density measurements have been made only for oxide films prepared at a substrate temperature of  $300^\circ\text{C}$ . The measured value is  $2.18 \text{ gms/cm}^3$  which compares favorably with the accepted value of  $2.21 \text{ gms/cm}^3$  for fused silica.

## 2. Aluminum Oxide

One area of considerable success in the program has been the deposition of aluminum oxide. Films with uniform thickness, uniform density and dielectric constant, and low pinhole densities have been achieved. In the interim report on this contract, we reported developing RF plasma deposited aluminum oxide which had the stoichiometry of  $\text{Al}_2\text{O}_3$  within the accuracy of our measurement technique (i.e.,  $\pm 2$  percent). During the latter half of 1973, our efforts have been devoted toward characterizing the physical properties of this insulator and developing techniques to make it technologically useful.

TABLE 3-2. NEUTRON ACTIVATION ANALYSIS IMPURITY CONCENTRATIONS

	Na	Cu	As	Sb	Au	Br	Ga
Units (atoms/cm <sup>3</sup> )	10 <sup>15</sup>	10 <sup>15</sup>	10 <sup>14</sup>	10 <sup>14</sup>	10 <sup>12</sup>	10 <sup>14</sup>	10 <sup>14</sup>
Detection Limits	0.1	0.3	0.05	0.05	1	0.1	0.4
SiN <sub>x</sub>							
Mean	13.7	3.6	0.28	0.95	<1	1.3	<0.4
Standard Deviation	3.9	2.4	0.12	0.46	—	0.4	—
Probable Error (68 percent)	2.6	1.6	0.08	0.31	—	0.3	—
SiO <sub>x</sub>							
Mean	26.5	28.8	0.80	0.14	<1	2.8	<0.4
Standard Deviation	7.1	16.9	0.18	0.09	—	0.7	—
Probable Error (68 percent)	4.8	11.4	0.12	0.06	—	0.5	—
Control Samples							
Mean	4.3	3.0	1.8	6.6	1.0	1.0	<0.4
Standard Deviation	4.7	1.3	2.2	9.8	0.4	0.9	—
Probable Error (68 percent)	3.2	0.9	1.5	6.1	0.3	0.6	—

These activities were not in general separable; for in order to be technologically useful, the properties of the insulator must be reproducible. Two measures we have chosen to evaluate the reproducibility of the insulator are index of refraction and low frequency dielectric constant. These properties are not, of course, independent. In fact, the index of refraction is merely the square root of the high frequency dielectric constant. In what follows, we shall concentrate on the static dielectric constant because it reflects not only electronic polarization but also ionic polarization and hence is expected to be a more sensitive measure.

Recalling that

$$\frac{\epsilon - 1}{\epsilon + 2} = \frac{1}{3} \gamma (A + \alpha) \quad (3-1)$$

where  $\epsilon$  is the static dielectric constant,  $\gamma$  a factor which depends on choice of units, and  $A$  and  $\alpha$  are the ionic and electronic polarizability per unit volume, respectively,<sup>10</sup> we can write

$$\epsilon_{DF} = \frac{2 \rho_{DF} (\epsilon_B + 2) + \rho_B (\epsilon_B - 1)}{\rho_B (\epsilon_B - 1) - \rho_{DF} (\epsilon_B - 1)} \quad (3-2)$$

where  $\epsilon_B$  and  $\epsilon_{DF}$  are the dielectric indices of the bulk and deposited film and  $\rho_B$  and  $\rho_{DF}$  are the densities. Navias<sup>11</sup> has measured the dielectric index of a pure Al<sub>2</sub>O<sub>3</sub> ceramic of density 3.788 to be 9.25. We have measured the density of plasma deposited aluminum oxide to vary from 2.4 g/cm<sup>3</sup> to 3.0 g/cm<sup>3</sup> as the temperature of the substrate during deposition was varied from 300°C to 550°C. If we choose 2.9 g/cm<sup>3</sup> as a typical value for material deposited at 400°C, we calculate, from Equation (3-2),  $\epsilon_{DF} = 4.82$ .

The dielectric constant of the insulator was determined from measurement of MIS capacitors biased with the semiconductor surface accumulated. Some care is necessary in this technique to ensure that the surface is really accumulated and that leakage current is not distorting the measured values of capacitance. Measurement on eight slices from two different depositions

yielded a mean value for the dielectric index of 4.66 with a variance of 0.31, a result in reasonable agreement with the calculated value. It should be pointed out that the variance in measured dielectric constant arises at least in part from variation in oxide thickness across a slice, since the thickness is typically measured at only one point on the slice where changes in interference color indicate that thickness variation of up to 10 percent may be seen over a distance of  $\sim 2$  cm on a slice.

It was recognized in the interim report that pinholes in the deposited insulators were a major obstacle to technological application of these films. As a result of this, a determined effort was undertaken to identify and eliminate the cause of these pinholes. It was established that, for the case of plasma deposited  $\text{Al}_x\text{O}_3$ , most of the pinholes were a result of contamination of the surface. It was further established that the procedure described in Table 3-3 drastically reduced the pinhole count.

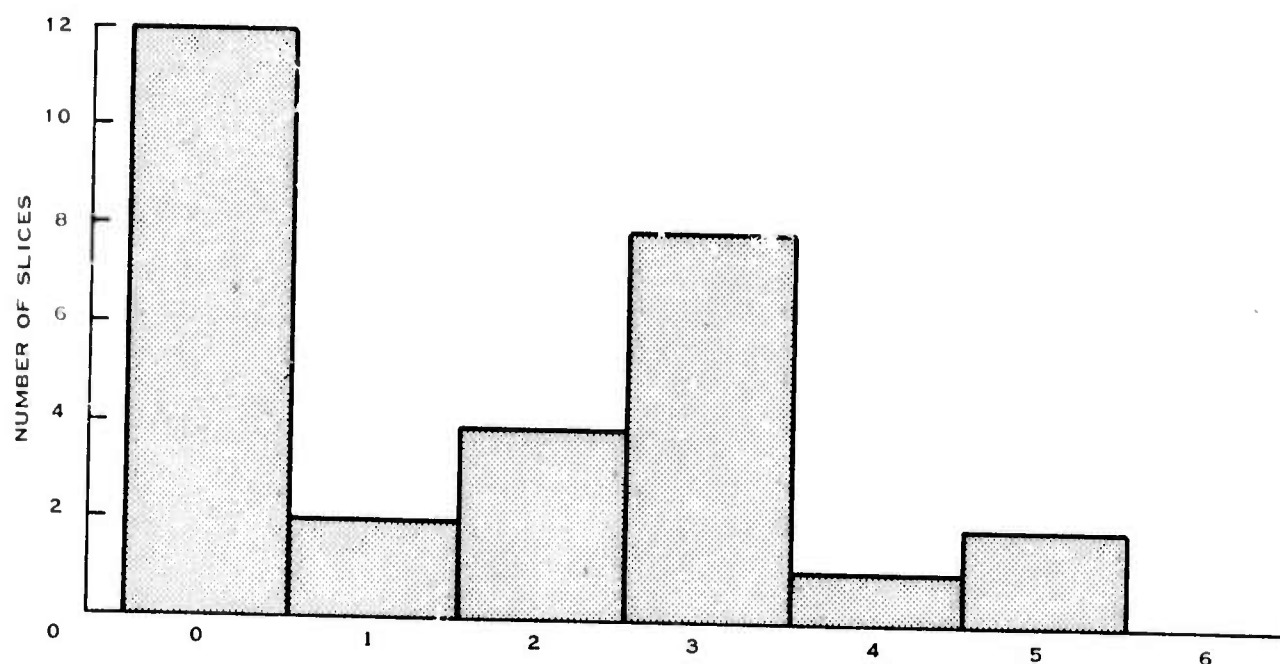
TABLE 3-3. SURFACE PREPARATION PROCEDURE

5 minutes boiling xylene	}	Remove organic contaminants
5 minutes boiling methanol		
5 minutes boiling isopropanol		
Rinse in de-ionized water		
Etch the semiconductor to remove $\sim 1 \mu\text{m}$ of material		
Rinse in de-ionized water for 30 minutes		
Blow the sample dry with filtered $\text{N}_2$ in a class 110 cleanroom		
Load the samples onto the graphite holder and place the holder into a sealed glass container while in cleanroom		
Slide the holder from the container into the deposition apparatus and immediately evacuate.		

Measurements of pinhole densities were performed, using a variety of techniques including scanning electron microscopy and selective etching, but the most reliable results were obtained using a "Navionic Dielectric Defect Detector." The apparatus consists of a gold-plated dish filled with methanol, to which the semiconductor slice makes contact. A copper ring is used as the anode and is placed 0.76 mm above the insulator surface. The semiconductor serves as the cathode of an electrophoretic cell so that, when a potential of about 1 volt is applied, preferential conduction occurs at any pinholes in the insulator, and gas bubbles evolve at these points. A microscope with calibrated grid is used to provide a count of pinholes per unit area. Translation controls are available so that an entire sample surface may be examined. Theoretically, pinholes as small as  $0.1 \mu\text{m}$  should be detectable with such a system.

The histogram in Figure 3-4 shows the pinhole densities per  $10 \text{ mm}^2$  measured on a number of slices after the above procedure was instituted. Note that zero pinholes indicates that no pinholes were found over an entire slice of  $\sim 3 \text{ cm}^2$  surface area. Thus, 41 percent of the slices in this sampling had no pinholes. These data are typical of those we have obtained since instituting this procedure and compare favorably with the state-of-the-art for thermally oxidized Si.

Ion backscattering analysis was used to determine the stoichiometry of the  $\text{AlO}_x$  films. Stoichiometric ratios of the deposited layers calculated from the backscattering analyses are given in Table 3-4 as a function of temperature and gas ratio. The accuracy of the stoichiometric ratios is 1 percent. The measured indices of refraction are also given. Note that the refractive index increases monotonically with increased value of the ratio  $[\text{Al}]/[\text{O}]$ . Note also that stoichiometric ratios cluster closely about the value 0.667 expected for aluminum oxide.



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Figure 3-4. Histogram of Pinhole Densities in AlO<sub>x</sub>

TABLE 3-4. STOICHIOMETRIC RATIOS OF THE DEPOSITED LAYER  
CALCULATED FROM BACKSCATTERING ANALYSES

TMA/N <sub>2</sub> O	1/10	1/20	1/40	1/80
Temperature				
560°C			[Al]/[O] = 0.739 n = 1.703	
400°C	[Al]/[O] = 0.675 n = 1.643	[Al]/[O] = 0.657 n = 1.593	[Al]/[O] = 0.691 n = 1.678	
290°C			[Al]/[O] = 0.633 n = 1.526	

#### D. LIQUID PHASE ANODIZATION

Anodization uses an electric field assisted reaction of oxygen with a solid to form an insulating oxide film. Extensive reviews of the subject are available.<sup>12,13</sup> Anodization has been studied extensively because of its importance in corrosion as well as in the fabrication of insulator films for electrical components. The first field-effect transistor ever fabricated used an anodic oxide film on Ge,<sup>14</sup> but subsequent success in the growth of thermal oxides on Si made anodization unnecessary.

For growth of insulators on compound semiconducting materials, however, anodization offers some distinct advantages:

- It is a low-temperature process; high-temperature processes lead to vaporization of the more volatile group V species in III-V compounds, causing surface damage and stoichiometric alterations in the semiconductor.
- It offers inherently self-healing film growth. Pinholes which may develop in the insulator become points of maximum electric field and are therefore eliminated by more rapid insulator growth.
- It eliminates the original semiconductor surface from the final MIS structure. This is an advantage over deposited insulators, where structural damage and contamination on the semiconductor surface lead to undesirable semiconductor-insulator interface properties.

Studies conducted during this program have used both liquids and plasma as the electrolytes for anodization. Plasma anodization offers the distinct advantage of freedom from impurity contamination, but is a more difficult process to control than liquid anodization. Although the use of a liquid electrolyte has been reported to result in deleterious electrical effects caused by incorporation of water and OH ions in the films,<sup>15</sup> methods are available for "baking-out" these contaminants; some anodic films show desirable insulator characteristics even without such a process.<sup>16</sup>

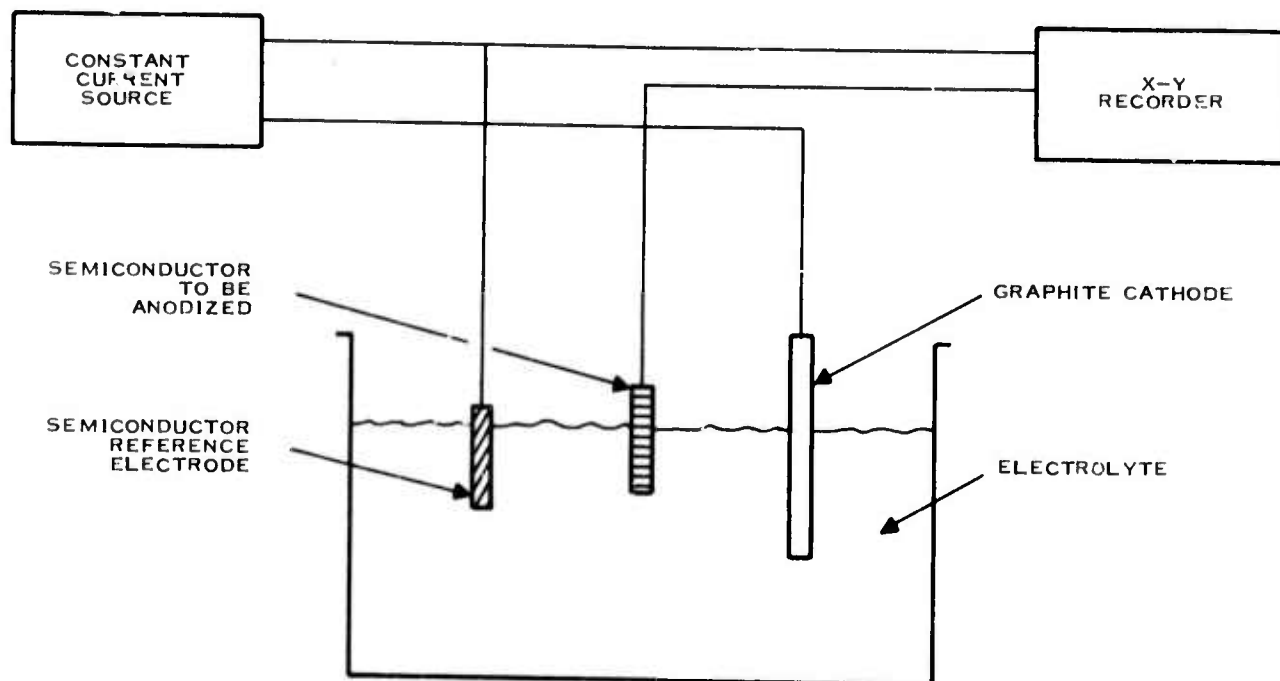
Anodization of semiconductors in oxidizing solutions has been reported for InSb,<sup>17</sup> GaAs,<sup>18</sup> and GaP.<sup>19</sup> The oxides formed on InSb in aqueous KOH solutions have been successfully used for field-effect devices.<sup>20</sup> This type of anodization is the principal technique used in Texas Instruments program, but a modification which has not been reported previously has been used with some success. In the modification, solutions containing anions other than oxygen (principally sulfur) have been used as electrolytes. Such an approach provides a variety of insulators, other than oxides, for evaluation in MIS structures.

The apparatus used for anodization is shown in Figure 3-5. The reference electrode serves to counterbalance the solution potential and is made of the same semiconductor material as the anode. The apparatus can be easily altered for operation at constant current, constant voltage, or programmed ramp voltage.

Water, glycerine, and ethylene glycol have been used as electrolyte solvents. The latter two are used in cases where anodization is to be done at large voltages, exceeding the decomposition potential of water. Most anodic oxidation has been performed on GaSb, GaInAs, and Ge, using approximately 0.1 N KOH dissolved in these solvents, although other oxidizing solutions, such as  $\text{NH}_4\text{OH}$  and  $\text{H}_2\text{O}_2$ , have also been used. Attempts to form sulfide films have been made with  $\text{Na}_2\text{S}$  and sulfurated  $\text{K}_2\text{CO}_3$  in the same solvents.

Variables that have been used to alter anodization characteristics include temperature, anodization time, current or voltage condition, solute concentration, and incident illumination.

Backsides of the semiconductor samples are normally masked during the anodization either with one of several types of photoresist or with black wax. Following anodization, the samples are rinsed in organic solvents and water, and then characterized, using optical microscopy, scanning electron microscopy, and dielectric-defect detection (pinholes). Metal dots are normally deposited on the insulator surface and the electrical characterization performed.



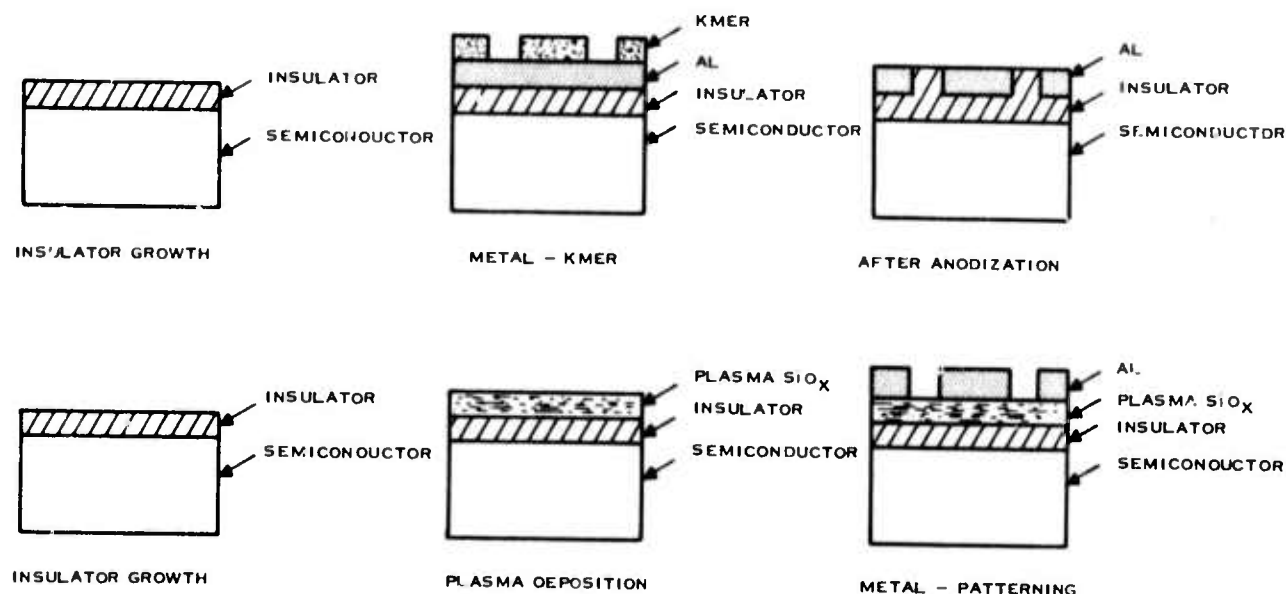
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Figure 3-5. Anodization Apparatus Wired for Constant Current Operation

The most notable results have been achieved on GaInAs using the 0.1 N KOH-ethylene glycol electrolyte, and on Ge using the sulfide solutions. Oxide films grown on GaInAs were reproducible, and showed few or no pinholes and less than  $\pm 3$  percent thickness variation. Capacitance-voltage measurements showed band bending in most cases and flatband voltages less than 1 volt, with a hysteresis of similar magnitude. Auger analysis indicated the presence of significant amounts of carbon in the anodic films, typically between 5 and 10 percent, in addition to the 30 percent oxygen present. Since film resistivities were less than  $10^{10}$  ohm-cm, a low breakdown strength was typical in these samples, and was not significantly improved by standard annealing treatments. It appears likely that the organic electrolyte is causing the carbon contamination. For this reason, further investigation of this oxide was discontinued in the hope that use of a plasma anodization process would maintain desirable cosmetic and electrical properties while eliminating electrolyte contaminants and increasing film resistivity and stability.

Films formed on Ge in the sulfide solutions showed flatband voltages less than 1 volt with little or no hysteresis in the best cases, and resistivities as high as  $10^{16}$  ohm-cm. These insulators degraded, however, after prolonged exposure to ambient conditions. In the better films, concentrations of approximately 3 percent each, of oxygen, nitrogen, and carbon, were found by Auger analysis.

Here, again, it was decided that further development could best be performed by using a plasma electrolyte to control impurity contamination and to provide protective insulator coatings that could be deposited *in situ* after anodization.



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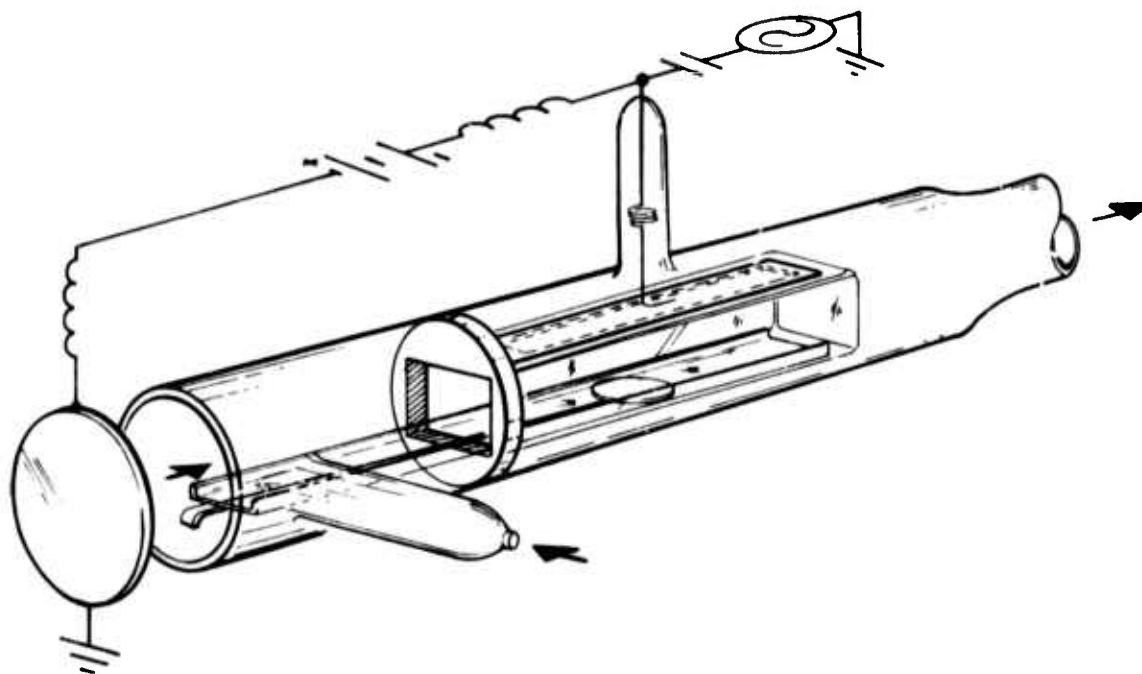
Figure 3-6. Planar Process Development

Most of the anodic films have shown no resistance to acid attack, thus making the patterning of Al for a surface planar process very difficult. Potassium iodide and potassium ferricyanide were used to pattern Al on some of the anodic films, but these etchants appear to degrade the electrical properties of the insulators. Planar processes were therefore developed for these materials. Two of the approaches are shown in Figure 3-6. In the first case, Al was deposited on the insulator surface and then anodized in selected areas, by using a photoresist mask, to produce the desired metallization pattern.

In the second case, a protective plasma-deposited  $\text{SiO}_x$  layer was used and then standard photoresist techniques were used to pattern the aluminum.

#### E. PLASMA ANODIZATION

Gaseous, or plasma, anodization has been used to produce many types of devices, including capacitors, Josephson junctions, MOS transistors, tunnel barriers, and others. A recent review of the process is given by Dell'Oca, Pulfrey, and Young.<sup>21</sup> Two different types of anodization methods in plasmas are readily distinguished. In the first, a dc discharge is established with an appropriate potential (this may be either a cold-cathode or a hot-cathode discharge). The material to be anodized is biased positively at a different voltage with respect to the plasma to supply the anodization current. In the second method, an oxygen plasma is created by a microwave discharge and the sample is placed in the afterglow, again with an appropriate bias. Both of these techniques appear to have serious problems. In the dc technique, high voltages are



164353

Figure 3-7. Diagram of Plasma Anodization Apparatus

necessary as is a three-electrode system. The many regions of a dc glow discharge require careful sample placement if reproducible results are to be obtained. Thus far, it appears as if a microwave-supported discharge is not capable of uniform processing over a large enough sample area to make it practical. A third method is that of using an RF-supported discharge to create the plasma, with additional dc biasing to supply the anodization current. This last technique is the one that has been investigated in this program. The experimental apparatus is shown schematically in Figure 3-7. It is a simple modification of the apparatus used for plasma chemical deposition. The conducting slice holder shown in Figure 3-2 is replaced with a quartz plate on the bottom of which a thin platinum wire is strung. At several points along the quartz, holes are drilled and the platinum wire is extended to the upper surface where it serves as a contact to the backside of a slice. When placed in the inner, rectangular cross-section tube, the platinum wire is shielded from the discharge by the quartz plate. A rectangular slot is cut into the upper section of the inner rectangular cross-section tube and an aluminum plate is used for the other electrode. A hole in this plate supports a platinum wire, which is brought to the top of plate and makes contact with the outside world through the spring electrode. The RF generator and the dc bias supply are isolated from each other by a filter network of passive circuit elements.

Growth of uniform films by plasma anodization was found to depend primarily upon application of the dc bias uniformly over the sample. This was accomplished by depositing gold over the entire backside of each sample and then using a silver paste to provide contact between the platinum wire and the sample. Two-inch slices of Si, anodized using this technique, showed less than  $\pm 3$  percent thickness uniformity over the entire slice. The film resistivity and

breakdown strength of the plasma-anodized  $\text{SiO}_x$  was comparable to thermally grown  $\text{SiO}_2$ , after annealing 30 minutes at  $450^\circ\text{C}$  in a nitrogen gas flow.

Capacitance voltage measurements typically show flatband voltages less than 2 volts and hysteresis less than 0.2 volt. Interface state densities, examined via conductance-voltage measurements (see Section IV), are in the  $3$  to  $5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  range.

Anodic oxidation of Ge in the plasma was followed by plasma deposition of  $200 \text{ \AA}$  of  $\text{SiO}_x$  to protect the insulator from ambient effects. These structures show more hysteresis than the anodized Si, being typically 1 volt, and show flatband voltages less than 2 volts and surface state densities in the  $3$  to  $5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  range after annealing. The  $\text{SiO}_x$  overcoat effectively protects the insulators from degradation caused by metal-patterning etches and ambient effects.

Attempts to grow nitride insulators by plasma anodization of Ge revealed that the solubility of  $\text{GeO}_x$  in water is eliminated if a few percent of nitrogen is incorporated in the material. Nitrogen gas and ammonia were both used as sources of nitrogen in attempts to produce insulators approximately  $\text{Ge}_3\text{N}_4$  in composition. Thus far, attempts to increase nitrogen content have resulted in films containing no more than 17 percent nitrogen, as determined by Auger analysis of the insulators after sputtering off several angstroms of the films.

Attempts to grow  $\text{GeS}_x$  compounds by plasma anodization, using a carbonyl sulfide gas flow, resulted in films with up to 12 percent S. This process causes deposition of elemental sulfur in the reactor, and some damage to the pumping system. Both the nitride and sulfide films exhibit some carbon and oxygen contamination.

## SECTION IV ELECTRICAL MEASUREMENTS

### A. GENERAL PRINCIPLES

Electrical characterization has been done chiefly by capacitance-voltage (C-V) and current-voltage (I-V) measurements on metal-insulator-semiconductor (MIS) capacitors. When the semiconductor is accumulated, the capacitance measured is that of only the insulator layer,

$$C_I = \frac{AK_I \epsilon_0}{X_I} \quad (4-1)$$

where  $A$  is the area of the metal contact,  $K_I$  is the dielectric constant of the insulator, and  $X_I$  is the insulator thickness. If the semiconductor is in inversion, the measured capacitance is the series combination of the insulator and the semiconductor depletion layer,

$$C_M = \frac{C_I C_S}{C_I + C_S} \quad (4-2)$$

The semiconductor capacitance is described by

$$C_S = \frac{AK_S \epsilon_0}{X_d} \quad (4-3)$$

where the depletion layer thickness for an inverted layer is

$$X_d = 2 \sqrt{\frac{K_S \epsilon_0 \phi_F}{q N_D}} \quad (4-4)$$

where  $K_S$  is the dielectric constant of the semiconductor,  $N_D$  is the net ionized dopant density and  $\phi_F$  is the potential difference between the Fermi level and the intrinsic Fermi level. Finally,

$$\phi_F = \frac{kT}{q} \ln \left( \frac{N_D}{n_i} \right) \quad (4-5)$$

if the semiconductor is not degenerate (the case of interest).

If the capacitance is measured with the semiconductor both in inversion and in accumulation, Equations (4-2) through (4-5) can be solved iteratively for  $N_D$  and  $\phi_F$ . That is,  $\phi_F$  can be guessed and the guess used in Equations (4-2) through (4-4) to calculate  $N_D$  which can then be substituted into Equation (4-5) to solve for  $\phi_F$ . The new value of  $\phi_F$  can then be used

to calculate  $N_D$ . Since  $\phi_F$  depends on  $N_D$  only logarithmically, this procedure rapidly converges to yield values for  $\phi_F$  and  $N_D$ .

Under this program, a computer program has been developed which, when given  $C_M$ ,  $C_I$ , and  $X_I$ , computes  $K_I$  and  $N_D$ . This value for  $N_D$  is then compared with the value measured before the insulator was deposited to check that inversion and accumulation of the semiconductor surface were indeed obtained.

As the semiconductor surface is driven from accumulation to inversion by a bias voltage on the gate metal, there is a point at which the bands in the semiconductor are flat (i.e., bent into neither accumulation nor inversion). The bias voltage at which this occurs is of great significance for both scientific and practical reasons.

It is known that the flat-band voltage,

$$V_{FB} = \Phi_{MS} - \frac{Q_{SS}}{C_o} - \frac{1}{C_o} \int_0^{X_I} \frac{X}{X_I} \rho(X) d(X) \quad (4-6)$$

where  $\Phi_{MS}$  is the difference in metal-semiconductor work functions,  $Q_{SS}$  is the sheet charge at the semiconductor-insulator interface,  $C_o$  is the insulator capacity, and  $\rho$  is the insulator charge distribution. Since  $\Phi_{MS}$  is usually known,  $V_{FB}$  is a measure of  $Q_{SS}$  and  $\rho$ . Thus,  $V_{FB}$  gives information concerning the insulator and its interface with the semiconductor.

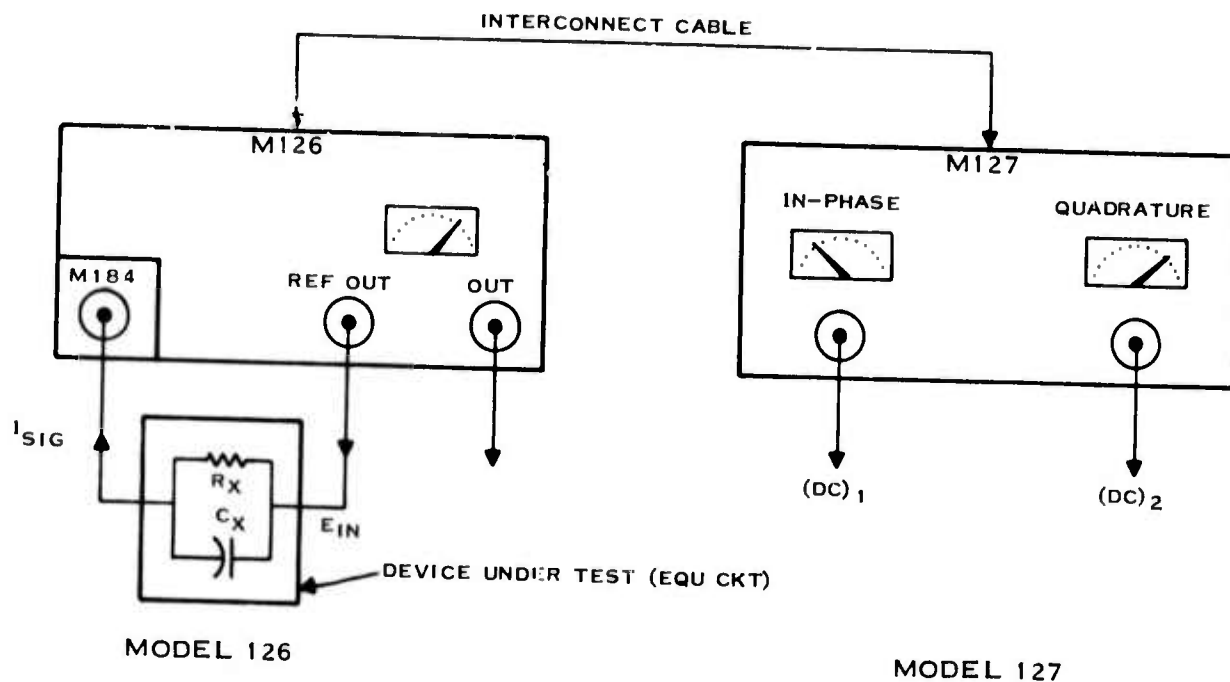
The precise determination of  $V_{FB}$  can be complicated in a device with a very large surface state density. However, a good estimate of  $V_{FB}$  can be made by simply comparing the measured high frequency C-V curves with the theoretical curves for an ideal device with the same insulator thickness, semiconductor substrate material, and doping. The translation of the experimental curve along the voltage axis from the position of the ideal curve provides a measure of the shift in  $V_{FB}$ .

Practically speaking, one would like to operate an MOS device at modest voltages. This requires  $V_{FB}$  to be small. From this point of view, measuring  $V_{FB}$  is monitoring an important device parameter. Moreover, from the device standpoint, one requires that  $V_{FB}$  be constant under repeated voltage cycling. Results from this type of measurement were reported in the June 1973 semiannual technical report for this contract.<sup>23</sup>

Electrical measurements are also used to determine the density of fast interface states. These states limit transfer efficiency in a CCD and contribute noise in other MOS devices. Measurements of interface state densities are much more difficult to perform and to analyze than those previously discussed, and they require an insulator with very low leakage and high stability. These measurements have received a great deal of attention recently in our program, and they are discussed in detail below.

## B. TEST FACILITIES

A considerable portion of our recent effort has been directed toward the development of a probe station facility to be used in the characterization of the insulators. This station is now



$$A \text{ CONDUCTANCE} = R_X^{-1} = \frac{(DC)_{OUT 1}}{E_{IN}} \times \frac{V_{FS}}{10\omega} \times \frac{(A/V)}{(PSD)} \text{ MHOS}$$

$$B \text{ CAPACITANCE} = C_X = \frac{(DC)_{OUT 2}}{E_{IN}} \times \frac{V_{FS}}{10} \times \frac{(A/V)}{(PSD)} \text{ FARADS}$$

#### DEFINITION OF TERMS

PSD = GAIN EXPANSION OF MIXER/DC AMPLIFIER (X1, 10, OR 100)

164365

Figure 4-1. Block Diagram of the Instrumentation of the Test Station

operative for measuring (1) capacitance-voltage characteristics using the Boonton C-V meter at 1 MHz, (2) capacitance-voltage and conductance-voltage characteristics from 50 Hz to 100 kHz using a Princeton Applied Research lock-in amplifier system, (3) current-voltage measurements for the determination of insulator leakage, (4) pulse capacitance measurements for use in determining bulk minority carrier lifetimes in processed slices, (5) variable-temperature operation of any of the above measurements using liquid nitrogen cooling and an electronic feedback control system which covers the temperature range from about 90 to 500°K. It is now possible to switch between these various measurements without removing the sample from the probe station. Within the next month, a computer will be added to the data acquisition system which will facilitate direct data input into the computer and detailed analysis by the computer.

The test instrument setup is relatively straightforward with the exception of the G-V and C-V measurement facility. This portion of the test setup is centered around the phase-sensitive detector (or lock-in amplifier) which is shown schematically in Figure 4-1. This system allows us

to measure the C-V and G-V characteristics simultaneously. The device under test is connected to a slowly swept dc bias voltage and a superimposed 10 mV rms signal from the reference oscillator output of the PAR amplifier. The substrate terminal of the MIS capacitor is then connected to the virtual ground input amplifier. Under these conditions, if the series resistance in the measurement circuit is sufficiently low, the outputs of the quadrature channels of the phase sensitive amplifiers are proportional G and  $\omega G$ , respectively. Series resistance in the measurement circuit limits the minimum values of conductance which can be measured. Such resistance may be in the input impedance of the current-to-voltage amplifier or in the bias network, or in the MIS device itself. Thus, series resistance also limits the minimum value of surface state density which can be measured accurately. Our system required the modification of the PAR equipment to reduce the output impedance of the reference oscillator below 50 ohms while still providing an adequate drive voltage for the measurement with no appreciable harmonic distortion. In most cases, the series resistance in the substrate is the dominant source of resistance in our measurements.

### C. SURFACE STATE MEASUREMENTS

The density of fast interface states is a very important property to determine in any of the MIS systems studies in this contract. We have devoted considerable effort in this area during this last 6-month period. Some of the effort has involved the assembly of the G-V and C-V test system and variable temperature apparatus. We have also taken C-V and G-V data on the insulators fabricated in this program.

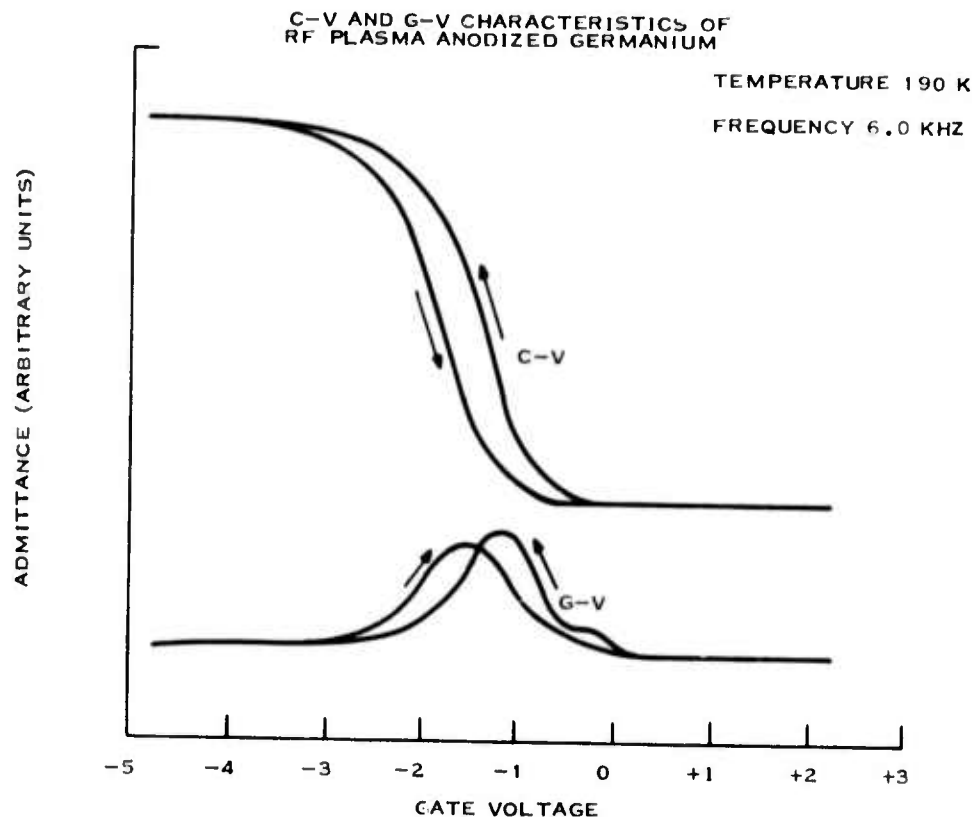
We have measured the G-V and C-V characteristics of Si-SiO<sub>2</sub>-Al devices as well, in order to test the system and to develop the measurement and analysis techniques. The principal advantage of the Si-SiO<sub>2</sub>-Al devices is their higher stability. In addition, their surface states have been studied more extensively making possible comparison to previous work. However, we feel that there is not yet an adequate general understanding of surface states even for the Si-SiO<sub>2</sub> interface, so that these efforts have complemented our studies in the other semiconductor insulator systems.

#### 1. Analysis of Surface State Densities in Silicon

Following the procedures outlined by Nicollian and Goetzberger and Dueling, et al.,<sup>24</sup> we can assume the circuit models shown in Figure 4-3 apply to our devices when biased in depletion. From the measured conductance,  $G_m$  and capacitance  $C_m$ , we can calculate

$$\frac{G_p}{\omega C_o} = \frac{G_m / \omega C_o}{(G_m / \omega C_o)^2 + (1 - C_m / C_o)^2} \quad (4-7)$$

$$\frac{G_p}{C_o} = \frac{1 - C_m / C_o}{(G_m / \omega C_o)^2 + (1 - C_m / C_o)^2} - 1 \quad (4-8)$$



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Figure 4-2. C-V and G-V Characteristics of RF Plasma Anodized Germanium

The conductance,  $G_p$ , is related to surface state density by

$$\frac{G_p}{\omega C_o} = \frac{qN_{ss}A}{C_{ox}} \int_{-\infty}^{\infty} \frac{\exp(-Z^2/2\sigma^2)}{\sqrt{2\pi}\sigma} \frac{\ln(1 + \omega^2\tau^2 e^{-2z})}{2\omega\tau e^{-z}} dZ \quad (4-9)$$

where  $N_{ss}$  is the density of surface states ( $\text{cm}^{-2} \text{ eV}^{-1}$ ),  $q$  is the electronic charge,  $A$  is the area of the device,  $\sigma^2$  is the variance of the fluctuations in surface potential,  $z$  is the deviation from the average surface potential in units of  $kT/q$ , and  $\tau$  is the relaxation time for filling and emptying the surface states lying within  $\pm kT/q$  of the surface potential corresponding to the applied bias.

Our general procedure is illustrated by an example of measurements and analysis on a Si/SiO<sub>2</sub>/Al device. First, C-V and G-V data were obtained at a number of frequencies between 100 Hz and 100 kHz as shown in Figure 4-4. From plots like Figure 4-3 we select a certain bias voltage in the depletion region and read the corresponding values of  $C$  and  $G$ . Then Equation 4-7 and Equation 4-8 are used to determine the corresponding values of  $G_p(\omega)$  and  $C_p(\omega)$ . Figure 4-5,  $G_p(\omega)/\omega C_o$  is plotted for this same device. Equation 4-9 is fitted to the experimental data by adjusting the parameters  $N_{ss}$ ,  $\sigma$ ,  $\tau$  using a least squares fitting routine on a computer. The resulting theoretical curve for this example is also shown in Figure 4-4. In this example, the calculated values of the mode parameters are

$$N_{SS} = 2.0 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$$

$$\sigma = 1.1$$

$$\tau = 6.1 \times 10^{-5} \text{ sec.}$$

This particular device has a very low surface state density which is near the lower limits of the resolution of our experimental equipment. When the surface state density is this low, we find the ratio  $G/\omega c$  to be on the order  $1 \times 10^{-3}$  which makes very high demands on the stability of the phase-sensitive detector. The effects of series resistance in the semiconductor also limit the accuracy of conductance measurements at high frequencies.

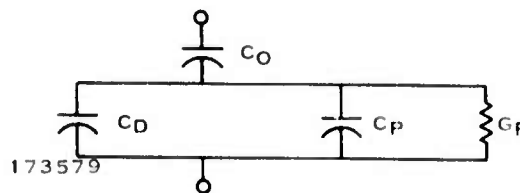


Figure 4-3. Equivalent Circuit for MIS Capacitor

## 2. Fast Interface State Measurements in Ge-AlO<sub>x</sub>-Al

The curves in Figure 4-2 represent C-V and GV data which were obtained from an RF plasma anodized Ge slice. These curves are also typical of data we have been obtaining from deposited aluminum oxide on germanium. The hysteresis observed in these curves is a serious problem in using these and other similar data for surface state density analysis. Another problem area in analyzing surface state densities on these devices is that of instabilities and hysteresis in the C-V and G-V curves. In some devices variations in the amount of hysteresis are observed from one measurement to the next. Also in some devices we see the whole curve translate along the voltage axis from one measurement to the next. Such instabilities make it impossible to

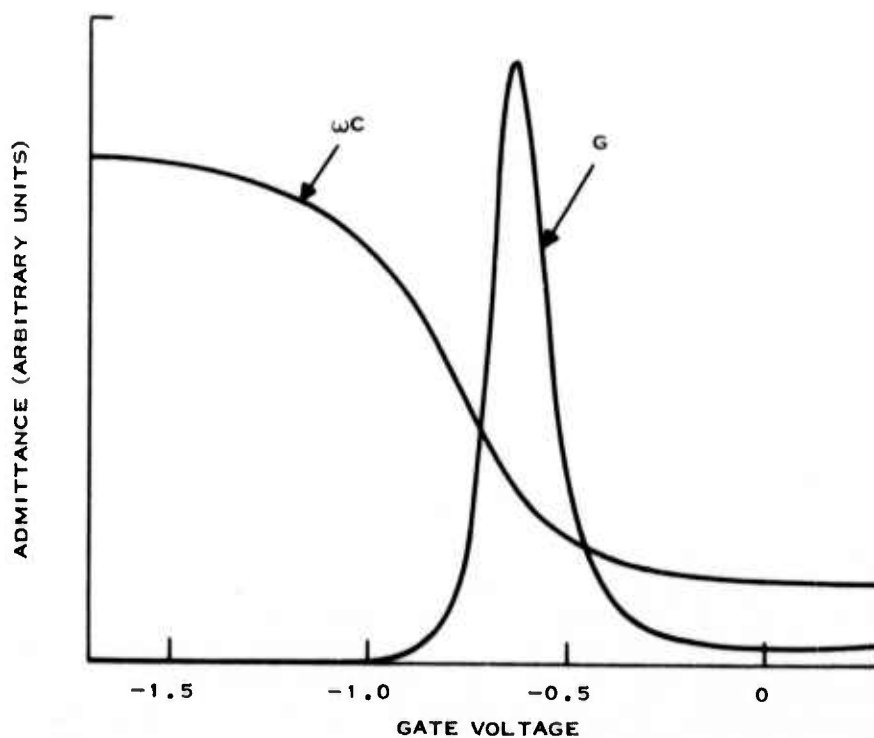


Figure 4-4. Typical C-V and G-V Characteristics of Al-SiO<sub>2</sub>-Si at 4.0 kHz

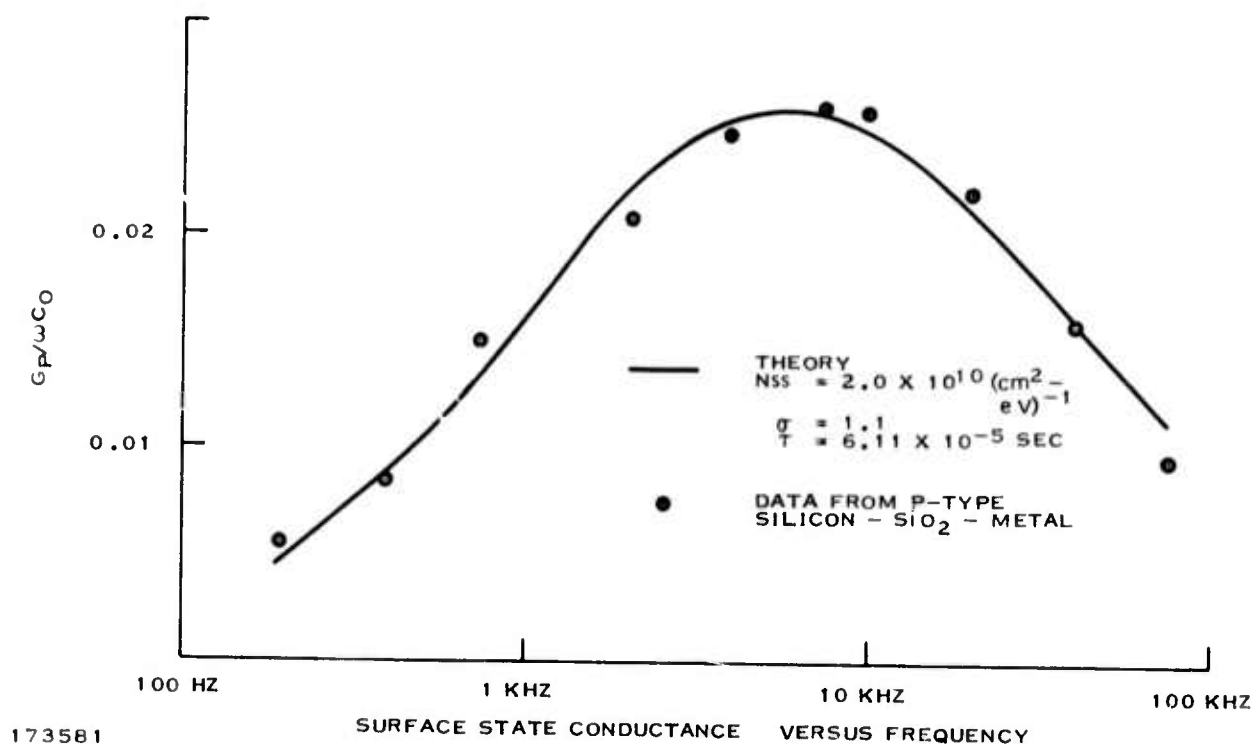


Figure 4-5. Surface State Conductance Versus Frequency

correlate measurements at different frequencies at the same bias voltage as we require for the analysis. However, we can still estimate from these data surface state densities in the midgap region without knowing exactly what energy level and time constant ( $\tau$ ) to associate with measurement and without knowing the statistical fluctuations ( $\sigma$ ) of the surface potential. This kind of estimate of surface state density based on magnitude of ( $G_p/\omega$ ) maximum at 4 kHz and 190 K leads to a value  $\sim 3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  for the RF plasma anodized germanium slice shown in Figure 4-2.

### 3. Insulator Electrical Instabilities

At this point in the program, it is not possible to determine the cause of the hysteresis and instabilities in our MIS structures. One possibility is the presence of highly mobile impurities in the insulator. Such impurities would vary on different slices as we have observed. Presumably, they could be eliminated with an appropriate step in the surface cleanup process before the insulator is deposited or grown. Another possibility might be that there is charge injection from the semiconductor into slow trapping states within the insulator. Such states might be unavoidable in some of the insulators. On the other hand, it may be possible to eliminate them in some cases by means of appropriate annealing steps in controlled atmospheres. We are currently investigating the effects of different cleanup procedures and annealing samples in gases such as  $\text{N}_2$ ,  $\text{H}_2$ ,  $\text{O}_2$ , and argon in attempts to lower interface state densities and to determine the feasibility of eliminating hysteresis and instabilities.

## SECTION V

### CONCLUSIONS

During this contract period, considerable progress has been made in preparing the (Ga,In)As samples. The dual-source reactor has produced graded alloys to help match the GaAs substrate to the epitaxial alloy film grown on it. Optimization of this new system is still in progress.

Preparation of thin insulator films has been done with reactive plasma depositions, plasma anodization, and liquid anodization. All of these are low-temperature techniques which avoid the problems associated with high-temperature processing of (Ga,In)As. Many of the pinhole problems in  $\text{AlO}_x$  have been solved by improved surface preparation techniques. Thus  $\text{AlO}_x$  appears to be the best overall insulator so far in this program. We are continuing to study the plasma anodization scheme as it has produced promising but inconsistent results.

Our electrical characterization facilities are now quite comprehensive. Complete electrical characterizations of the insulators depends on achieving stable, low-leakage, and pinhole-free films factors which have not always allowed the determination of breakdown strengths and surface state densities. The final phase of this program should provide more extensive electrical data on our better insulating films.

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**APPENDIX A**  
**INSULATOR-SEMICONDUCTOR STRUCTURES PREPARED IN THE PROGRAM**

Sample Number	Substrate	Insulator	Comment	Film Thickness (Å)	Index of Refraction
Si-12-5-1-A	Si	SiO <sub>2</sub>	Control Sample	1088	1.4777
Si-12-5-1-B	Si	SiO <sub>2</sub>	Control Sample	1131	1.4809
Si-12-5-2	Si	SiO <sub>2</sub>	Control Sample	1075	1.480
GaSb-12-5-2-A	GaSb	SiO <sub>2</sub>	p = 2.5 × 10 <sup>17</sup>	1131	1.475
GaSb-12-5-2-B	GaSb	SiO <sub>2</sub>		1137	1.474
GaSb-12-12-1	GaSb	Si <sub>3</sub> N <sub>4</sub>	Predeposition clean in N <sub>2</sub> discharge	962	1.98
GaSb-12-12-2	GaSb	Si <sub>3</sub> N <sub>4</sub>	No preclean	955	2.00
Si-12-12-1	Si	Si <sub>3</sub> N <sub>4</sub>	Predeposition clean in N <sub>2</sub> discharge		
Si-12-12-2	Si	Si <sub>3</sub> N <sub>4</sub>	No preclean	938	1.99
GaInAs-12-12-1	Ga <sub>0.65</sub> In <sub>0.35</sub> As	Si <sub>3</sub> N <sub>4</sub>	Predeposition clean in N <sub>2</sub> discharge		
GaSb 1-5-2-A	GaSb	SiN <sub>x</sub>	Final rinse in D.I. H <sub>2</sub> O	~1000	
GaSb 1-5-2-B	GaSb	SiN <sub>x</sub>	Final rinse in Transene 100	~1000	
Si 1-5-2-A	Si	SiN <sub>x</sub>	Control sample	~1000	
GaAs 1-10-4-A	GaAs	SiO <sub>x</sub> , SiN <sub>x</sub>	Double-layer insulator	~200 Å SiO <sub>x</sub> ~800 Å SiN <sub>x</sub>	
GaAs 1-10-4-B	GaAs	SiN <sub>x</sub>		~1000	
InSb 1-11-10	InSb	Anodized	Liquid anodization test	~1500	
InSb 1-11-11	InSb	Anodized	Liquid anodization test	~800	
Ge 1-23-1-A	Ge	SiN <sub>x</sub>		641	1.97
Si 1-23-1-B	Si	SiN <sub>x</sub>		641	1.97
Si 1-23-1-D	Si	SiN <sub>x</sub>	Control sample (10-15 Ω cm)	641	1.97
Ge 1-23-2-A	Ge	SiO <sub>x</sub>	Control sample (1 Ω cm)	743	1.46
Si 1-23-2-B	Si	SiO <sub>x</sub>	Control sample	743	1.46
GaSb 1-23-3-A	GaSb	SiO <sub>x</sub>	Ultra-thin film test	251	1.46
Si 1-23-3-B	Si	SiO <sub>x</sub>	Control sample	251	1.46
GaSb-2-23-15	GaSb	GaSbS <sub>x</sub>	Anodized		
GaInAs-2-6-11	GaInAs	GaInAsO <sub>x</sub>	Anodized		
GaInAs-2-8-3	GaInAs	SiO <sub>x</sub>	Plasma etch cleaning	~800	
GaInAs-2-8-4	GaInAs	SiO <sub>x</sub> -SiN <sub>x</sub>	Plasma etch cleaning	~200; ~600	
GaInAs-2-13-11	GaInAs	GaInAsO <sub>x</sub>	Anodized	~1000	
GaInAs-2-13-12	GaInAs	GaInAsO <sub>x</sub>	Anodized	~500	

Sample Number	Substrate	Insulator	Comment	Film Thickness (Å)	Index of Refraction
GaInAs-2-14-10	GaInAs	GaInAsO <sub>x</sub>	Anodized	~1600	-
GaInAs-2-14-11	GaInAs	GaInAsO <sub>x</sub>	Anodized	~ 400	-
GaAs-2-8-3-A	GaAs	SiO <sub>x</sub>	Plasma etch cleaning	~ 800	-
Si-2-2-2	Si	Polymer Insulator	Plasma deposition	~1200	-
Si-2-6-2	Si	SiO <sub>x</sub>		862	1.493
Si-2-6-3	Si	SiO <sub>x</sub>	CF <sub>4</sub> plasma etch cleaning	827	1.535
Si-2-8-3	Si	SiO <sub>x</sub>	CF <sub>4</sub> plasma etch cleaning	800	~1.5
Si-2-8-4	Si	SiO <sub>x</sub> SiN <sub>x</sub>	Double layer structure	200; 600	-
Si-2-9-13	Si	SiO <sub>x</sub>	Plasma anodization	-	-
Si-GEP-13 No. 7	Si	SiO <sub>x</sub>	300°C Plasma	875	-
Si-GEP-13 No. 8	Si	SiO <sub>x</sub>	300°C Plasma	1050	-
Si-GEP-13 No. 2	Si	SiO <sub>x</sub>	300°C Plasma	1050	-
Si-GEP-13 No. 1	Si	SiO <sub>x</sub>	300°C Plasma	1000	-
Si-GEP-13 No. 4	Si	SiO <sub>x</sub>	300°C Plasma	875	-
Si-GEP-13 No. 5	Si	SiO <sub>x</sub>	300°C Plasma	1000	-
Si-GEP-12 No. 2	Si	SiO <sub>x</sub>	300°C Plasma-CF <sub>4</sub> etch	1250	-
Si-GEP-12 No. 4	Si	SiO <sub>x</sub>	300°C Plasma-CF <sub>4</sub> etch	1125	-
Si-GEP-12 No. 5	Si	SiO <sub>x</sub>	300°C Plasma-CF <sub>4</sub> etch	1000	-
Si-GEP-12 No. 7	Si	SiO <sub>x</sub>	300°C Plasma-CF <sub>4</sub> etch	1250	-
Si-GEP-12 No. 8	Si	SiO <sub>x</sub>	300°C Plasma-CF <sub>4</sub> etch	1100	-
GaInAs-3-7-10	Ga <sub>0.2</sub> In <sub>0.8</sub> As	GaInAsS <sub>x</sub>	Anodized	725	-
GaInAs-3-7-11	Ga <sub>0.2</sub> In <sub>0.8</sub> As	GaInAsS <sub>x</sub>	Anodized	375	-
GaInAs-3-8-1-B	Ga <sub>0.2</sub> In <sub>0.8</sub> As	SiO <sub>x</sub>	Plasma	~ 800	-
GaInAs-3-8-1-B	Ga <sub>0.2</sub> In <sub>0.8</sub> As	SiO <sub>x</sub>	Plasma	~ 800	-
GaInAs-3-22-10	Ga <sub>0.2</sub> In <sub>0.8</sub> As	GaInAsO <sub>x</sub>	Plasma anodized	-	-
GaSb-4-3-10	GaSb	GaSbO <sub>x</sub>	Anodized	~7000	-
GaSb-4-3-11	GaSb	GaSbO <sub>x</sub>	Anodized	~7000	-
GaSb-4-9-10	GaSb	GaSbO <sub>x</sub>	Anodized	-	-
GaSb-4-9-11	GaSb	GaSbO <sub>x</sub>	Anodized	-	-
GaSb-4-9-18	GaSb	GaSbO <sub>x</sub>	Anodized	-	-

Sample Number	Substrate	Insulator	Comment	Film Thickness (Å)	Index of Refraction
GaSb-4-9-19	GaSb	GaSbO <sub>x</sub>	Anodized	-	-
GaSb-4-9-20	GaSb	GaSbO <sub>x</sub>	Anodized	-	-
GaSb-4-9-3-A	GaSb	SiO <sub>x</sub>	Plasma	275	-
GaSb-4-9-3-B	GaSb	SiO <sub>x</sub>	Plasma	275	-
GaSb-4-10-10	GaSb	GaSbO <sub>x</sub>	Anodized	-	-
GaSb-4-10-11	GaSb	GaSbO <sub>x</sub>	Anodized	-	-
GaSb-4-10-12	GaSb	GaSbO <sub>x</sub>	Anodized	-	-
GaSb-4-26-1-A	GaSb	SiO <sub>x</sub>	Plasma	309	-
GaSb-4-26-1-B	GaSb	SiO <sub>x</sub>	Plasma	300	-
GaSb-4-26-1-C	GaSb	SiO <sub>x</sub>	Plasma	298	-
GaSb-4-26-1-D	GaSb	SiO <sub>x</sub>	Plasma	292	-
Si-4-3-1	Si	SiN <sub>x</sub>	Plasma	~1000	-
Si-4-3-2	Si	SiN <sub>x</sub>	Plasma	~2000	-
Si-4-3-3	Si	SiN <sub>x</sub>	Plasma	~3000	-
Si-4-3-4	Si	SiN <sub>x</sub>	Plasma	~4000	-
Si-4-3-5	Si	SiO <sub>x</sub>	Plasma	~1000	-
Si-4-3-6	Si	SiO <sub>x</sub>	Plasma	~2000	-
Si-4-3-7	Si	SiO <sub>x</sub>	Plasma	~3000	-
Si-4-3-8	Si	SiO <sub>x</sub>	Plasma	~4000	-
Si-4-19-1-C	Si	SiO <sub>x</sub>	Plasma	1063	-
Si-4-19-3-D	Si	SiO <sub>x</sub> -SiN <sub>x</sub>	Plasma	1098	-
Si-4-19-2-D	Si	SiO <sub>x</sub>	Plasma	2170	-
Si-4-19-4-D	Si	SiO <sub>x</sub>	Plasma	1192	-
GaInAs-4-3-12	Ga <sub>0.5</sub> In <sub>0.5</sub> As	GaInAsO <sub>x</sub>	Anodized	875	-
GaInAs-4-3-13	Ga <sub>0.5</sub> In <sub>0.5</sub> As	GaInAsO <sub>x</sub>	Anodized	1000	-
GaInAs-4-3-14	Ga <sub>0.5</sub> In <sub>0.5</sub> As	GaInAsO <sub>x</sub>	Anodized	300	-
GaInAs-4-3-15	Ga <sub>0.5</sub> In <sub>0.5</sub> As	GaInAsO <sub>x</sub>	Anodized	300	-
GaInAs-4-9-12	Ga <sub>0.5</sub> In <sub>0.5</sub> As	GaInAsO <sub>x</sub>	Anodized	-	-
GaInAs-4-9-13	Ga <sub>0.5</sub> In <sub>0.5</sub> As	GaInAsO <sub>x</sub>	Anodized	314	-
GaInAs-4-9-14	Ga <sub>0.5</sub> In <sub>0.5</sub> As	GaInAsO <sub>x</sub>	Anodized	725	-
GaInAs-4-9-15	Ga <sub>0.5</sub> In <sub>0.5</sub> As	GaInAsO <sub>x</sub>	Anodized	-	-

Sample No.	Substrate	Insulator	Comment	Film Thickness (Å)	Index of Refraction
GaInAs-4-9-16	Ga <sub>0.5</sub> In <sub>0.5</sub> As	GaInAsO <sub>x</sub>	Anodized	—	—
GaInAs-4-9-17	Ga <sub>0.5</sub> In <sub>0.5</sub> As	GaInAsO <sub>x</sub>	Anodized	—	—
GaInAs-4-9-4-A	Ga <sub>0.5</sub> In <sub>0.5</sub> As	SiO <sub>x</sub>	Plasma	785	—
GaInAs-4-9-4-B	Ga <sub>0.5</sub> In <sub>0.5</sub> As	SiO <sub>x</sub>	Plasma	785	—
GaInAs-4-10-13	Ga <sub>0.5</sub> In <sub>0.5</sub> As	GaInAsO <sub>x</sub>	Anodized	—	—
GaInAs-4-10-14	Ga <sub>0.5</sub> In <sub>0.5</sub> As	GaInAsO <sub>x</sub>	Anodized	—	—
GaInAs-4-10-15	Ga <sub>0.5</sub> In <sub>0.5</sub> As	GaInAsO <sub>x</sub>	Anodized	—	—
GaInAs-4-10-16	Ga <sub>0.5</sub> In <sub>0.5</sub> As	GaInAsO <sub>x</sub>	Anodized	—	—
GaInAs-4-10-17	Ga <sub>0.5</sub> In <sub>0.5</sub> As	GaInAsO <sub>x</sub>	Anodized	—	—
GaInAs-AlO <sub>x</sub> -27-1A	Ga <sub>0.5</sub> In <sub>0.5</sub> As	AlO <sub>x</sub>	Plasma	~1600	—
GaInAs-AlO <sub>x</sub> -28-1A	Ga <sub>0.5</sub> In <sub>0.5</sub> As	AlO <sub>x</sub>	Plasma	~1600	—
GaInAs-AlO <sub>x</sub> -27-1B	Ga <sub>0.5</sub> In <sub>0.5</sub> As	AlO <sub>x</sub>	Plasma	~1600	—
GaInAs-AlO <sub>x</sub> -28-1B	Ga <sub>0.5</sub> In <sub>0.5</sub> As	AlO <sub>x</sub>	Plasma	~1600	—
GaInAs-AlO <sub>x</sub> -28-1C	Ga <sub>0.5</sub> In <sub>0.5</sub> As	AlO <sub>x</sub>	Plasma	~1600	—
GaInAs-AlO <sub>x</sub> -27-1C	Ga <sub>0.5</sub> In <sub>0.5</sub> As	AlO <sub>x</sub>	Plasma	~1600	—
Si-5-9-1-A	Si	SiO <sub>x</sub>	Plasma anodized	~5000	—
Si-5-9-1-B	Si	SiO <sub>x</sub>	Plasma anodized, then etched	~1500	—
Si-5-9-1-C	Si	SiO <sub>x</sub>	Plasma anodized	~5000	—
Si-5-11-10	Si	SiO <sub>x</sub> -AlO <sub>x</sub>	Plasma SiO <sub>x</sub> -liquid-anodized Al	—	—
Si-5-11-11	Si	SiO <sub>x</sub> -AlO <sub>x</sub>	Plasma SiO <sub>x</sub> -liquid-anodized Al	—	—
Si-5-1-3	Si	SiN <sub>x</sub>	Plasma	234	—
Si-AlO <sub>x</sub> -27-2	Si	AlO <sub>x</sub>	Plasma	~ 800	—
Si-AlO <sub>x</sub> -27-1	Si	AlO <sub>x</sub>	Plasma	1800	—
Si-AlO <sub>x</sub> -28-1	Si	AlO <sub>x</sub>	Plasma	1700	—
Si-AlO <sub>x</sub> -28-2	Si	AlO <sub>x</sub>	Plasma	1400	—
Si-AlO <sub>x</sub> -28-3	Si	AlO <sub>x</sub>	Plasma	1600	—
Si-5-22-3-A	Si	SiO <sub>x</sub>	Plasma	764	—
Si-5-22-3-B	Si	SiO <sub>x</sub>	Plasma	1607	—
Si-5-22-3-C	Si	SiN <sub>x</sub>	Plasma	691	—

Sample Number	Substrate	Insulator	Comment	Film Thickness (Å)	Index of Refraction
Si-5-22-3-D	Si	SiN <sub>x</sub>	Plasma	1100	-
Si-5-23-6-A	Si	SiO <sub>x</sub>	Plasma	807	-
Si-5-23-6-B	Si	SiO <sub>x</sub>	Plasma	1628	-
Si-5-23-6-C	Si	SiN <sub>x</sub>	Plasma	752	-
Si-5-23-6-D	Si	SiN <sub>x</sub>	Plasma	1137	-
Si-6-19-6-A	Si	SiO <sub>x</sub>	Plasma	1154	-
Si-6-19-6-B	Si	SiO <sub>x</sub>	Plasma	1137	-
Si-6-25-2-A	Si	SiO <sub>x</sub>	Plasma	700	-
Si-6-25-2-B	Si	SiO <sub>x</sub>	Plasma, then liquid anodizing seal	700	-
Si-6-25-2-C	Si	SiO <sub>x</sub>	Plasma, then liquid anodizing seal	700	-
Si-6-25-2-D	Si	SiO <sub>x</sub>	Plasma, then liquid anodizing seal, then bake	700	-
Si-7-3-1-A	Si	SiO <sub>x</sub>	Plasma, then liquid anodizing seal, then bake	~ 700	-
Si-7-3-1-B	Si	SiO <sub>x</sub>	Plasma, then liquid anodizing seal, then bake	~ 700	-
Si-7-3-1-C	Si	SiO <sub>x</sub>	Plasma, then liquid anodizing seal, then bake	~ 700	-
Si-7-3-1-D	Si	SiO <sub>x</sub>	Plasma	~ 700	-
Si-7-3-1-A	Si	SiO <sub>x</sub>	Plasma	718	-
Si-7-3-1-B	Si	SiO <sub>x</sub>	Plasma	718	-
Si-7-3-1-C	Si	SiO <sub>x</sub>	Plasma	718	-
Si-7-3-1-D	Si	SiO <sub>x</sub>	Plasma	718	-
Si-A <sub>2</sub> O <sub>3</sub> -35A-1	Si	A <sub>2</sub> O <sub>3</sub>	Plasma	942	-
Si-A <sub>2</sub> O <sub>3</sub> -35B-3	Si	A <sub>2</sub> O <sub>3</sub>	Plasma	1048	-
Si-A <sub>2</sub> O <sub>3</sub> -35C-4	Si	A <sub>2</sub> O <sub>3</sub>	Plasma	1114	-
Si-7-17-1A	Si	SiN <sub>x</sub>	Plasma, then anodic seal	675	-
Si-7-17-1B	Si	SiN <sub>x</sub>	Plasma, then anodic seal	675	-
Si-7-17-2A	Si	SiO <sub>x</sub>	Plasma, then anodic seal	717	-
Si-7-17-2B	Si	SiO <sub>x</sub>	Plasma, then anodic seal	717	-
Si-7-18-3	Si	SiN <sub>x</sub>	Plasma	700	-
Si-7-19-3	Si	SiN <sub>x</sub>	Plasma, then anodic seal	700	-

Sample Number	Substrate	Insulator	Comment	Film Thickness (Å)	Index of Refraction
Si-7-20-10	Si	SiO <sub>x</sub>	Thermal oxide control	921	-
Si-7-20-11	Si	SiO <sub>x</sub>	Thermal oxide control	918	-
Si-7-19-1P	Si	SiO <sub>x</sub>	Plasma anodized	700	-
Si-7-19-2P	Si	SiO <sub>x</sub>	Plasma anodized	700	-
Si-7-19-3P	Si	SiO <sub>x</sub>	Plasma anodized	700	-
Si-7-23-1P	Si	SiO <sub>x</sub>	Plasma anodized	571	-
Si-7-23-2P	Si	SiO <sub>x</sub>	Plasma anodized	624	-
GaInAs-7-24-10	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Anodized	~1200	-
GaInAs-7-24-11	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Anodized	~1200	-
GaInAs-7-24-12	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Anodized	~1200	-
GaInAs-7-24-13	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Anodized	~1200	-
GaInAs-7-24-14	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Anodized	~500	-
GaInAs-7-24-15	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Anodized	~900	-
GaInAs-7-24-16	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Anodized	~1200	-
GaInAs-7-24-17	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Anodized	~600	-
GaInAs-8-28-10A	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Anodized	~600	-
GaInAs-8-28-10B	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Anodized	~600	-
GaInAs-9-10-10	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Poor film	-	-
GaInAs-9-10-11	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Poor film	-	-
GaInAs-9-10-12	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Anodized	~1200	-
GaInAs-9-10-13	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Anodized	~1200	-
GaInAs-9-10-14	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Not uniform	~900	-
GaInAs-9-10-15	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Anodized	~1100	-
GaInAs-10-6-1P	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Plasma anodized, not uniform	-	-
GaInAs-11-8-10	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Anodized	~1100	-
GaInAs-11-8-11	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Anodized	~1100	-
GaInAs-11-13-10	GaInAs	GaInAs <sub>2</sub> O <sub>x</sub>	Anodized	~1100	-
Ge-8-7-73P	Ge	GeO <sub>x</sub>	Plasma anodized	-	-
Ge-8-8-73P	Ge	GeO <sub>x</sub>	Plasma anodized	-	-
Ge-8-9-1P	Ge	GeO <sub>x</sub>	Plasma anodized	-	-
Ge-8-24-1PA	Ge	GeO <sub>x</sub> N <sub>y</sub>	Plasma anodized	-	-

Sample Number	Substrate	Insulator	Comment	Film Thickness (Å)	Index of Refraction
Ge-8-24-1PB	Ge	GeO <sub>x</sub> N <sub>y</sub>	Plasma anodized		
Ge-8-24-2P-A	Ge	GeO <sub>x</sub> N <sub>y</sub>	Plasma anodized		
Ge-8-24-2P-B	Ge	GeO <sub>x</sub> N <sub>y</sub>	Plasma anodized		
Ge-8-15-1P	Ge	GeO <sub>x</sub>	Plasma Anodized		
Ge-8-15-2P	Ge	GeO <sub>x</sub>	Plasma Anodized		
Ge-8-28-1P	Ge	GeO <sub>x</sub>	Plasma Anodized		
Ge-9-29-1P	Ge	GeO <sub>x</sub> N <sub>y</sub>	Plasma anodized		
Ge-10-2-1P	Ge	GeO <sub>x</sub> N <sub>y</sub>	Plasma Anodized		
Ge-10-2-2P	Ge	GeO <sub>x</sub> N <sub>y</sub>	Plasma Anodized		
Ge-10-2-3P	Ge	GeO <sub>x</sub> N <sub>y</sub>	Plasma Anodized		
Ge-10-11-1P	Ge	GeO <sub>x</sub>	Plasma Anodized		
Ge-10-11-1P	Ge	GeO <sub>x</sub>	Plasma Anodized		
Ge-10-25-1P	Ge	GeO <sub>x</sub>	Plasma Anodized		

**APPENDIX B**  
**INSULATOR-SEMICONDUCTOR STRUCTURES**  
**DELIVERED TO NVL FOR EVALUATION**

Sample No.	Semiconductor	Insulator	Insulator Thickness (Å)	Index of Refraction
GaSb 1-23-3-A	GaSb	SiO <sub>x</sub>	251	-
Si 1-23-3-B	Si	SiO <sub>x</sub>	251	-
GaSb 2-7-4-A	GaSb	SiN <sub>x</sub>	216	-
Si 2-7-4-A	Si	SiN <sub>x</sub>	216	-
Si 12-1-10	Si	AlO <sub>x</sub>	1310	-
GaInAs 12-12-i	Ga <sub>0.87</sub> In <sub>0.13</sub> As	SiN <sub>x</sub>	984	-
GaSb 1-5-2-A	GaSb	SiN <sub>x</sub>	1041	-
GaSb 12-12-1	GaSb	SiN <sub>x</sub>	962	-
Ge 2-12-10	Ge	SiO <sub>x</sub>	1150	-
GaSb 3-8-1-A	GaSb	SiO <sub>x</sub>	210	-
GaSb 3-8-2-A	GaSb	SiO <sub>x</sub>	817	-
GaSb 3-9-4-A	GaSb	SiN <sub>x</sub>	259	-
GaSb 3-9-5-A	GaSb	SiN <sub>x</sub>	894	-
GaInAs 3-8-1-B	Ga <sub>0.72</sub> In <sub>0.28</sub> As	SiO <sub>x</sub>	210	-
GaInAs 2-8-3	Ga <sub>0.7</sub> In <sub>0.3</sub> As	SiO <sub>x</sub>	773	-
GaInAs 3-9-4-B	Ga <sub>0.72</sub> In <sub>0.28</sub> As	SiN <sub>x</sub>	259	-
GaInAs 3-9-5-B	Ga <sub>0.72</sub> In <sub>0.28</sub> As	SiN <sub>x</sub>	894	-
GaInAs 4-9-13	Ga <sub>0.5</sub> In <sub>0.5</sub> As	GaInAsO <sub>x</sub>	314	-
GaInAs 4-9-14	Ga <sub>0.5</sub> In <sub>0.5</sub> As	GaInAsO <sub>x</sub>	725	-
GaInAs 4-9-4-A	Ga <sub>0.5</sub> In <sub>0.5</sub> As	SiO <sub>x</sub>	785	-
GaInAs 4-9-4-B	Ga <sub>0.5</sub> In <sub>0.5</sub> As	SiO <sub>x</sub>	785	-
GaSb 2-7-4-B	GaSb	SiN <sub>x</sub>	219	-
GaSb 1-5-2-B	GaSb	SiN <sub>x</sub>	1041	-
GaSb 4-9-3-A	GaSb	SiO <sub>x</sub>	275	-
GaSb 4-9-3-B	GaSb	SiO <sub>x</sub>	275	-
Si-AlO <sub>x</sub> -27-1	Si	AlO <sub>x</sub>	1800	-
Si-AlO <sub>x</sub> -28-1	Si	AlO <sub>x</sub>	1700	-
Si-AlO <sub>x</sub> -28-2	Si	AlO <sub>x</sub>	1400	-
Si-AlO <sub>x</sub> -28-3	Si	AlO <sub>x</sub>	1600	-
GaSb 4-26-1-A	GaSb	SiO <sub>x</sub>	309	-
GaSb 4-26-1-B	GaSb	SiO <sub>x</sub>	300	-
GaSb 4-26-1-C	GaSb	SiO <sub>x</sub>	298	-
GaSb 4-26-1-D	GaSb	SiO <sub>x</sub>	292	-

Sample No.	Semiconductor	Insulator	Insulator Thickness (Å)	Index of Refraction
Si-5-22-3-A	Si	SiO <sub>x</sub>	764	1.47
Si-5-22-3-B	Si	SiO <sub>x</sub>	1007	1.43
Si-5-23-6-A	Si	SiO <sub>x</sub>	807	1.47
Si-5-23-6-B	Si	SiO <sub>x</sub>	1628	1.43
Si-5-22-3-C	Si	SiN <sub>x</sub>	691	1.99
Si-5-22-3-D	Si	SiN <sub>x</sub>	1109	2.00
Si-5-23-6-C	Si	SiN <sub>x</sub>	752	1.96
Si-5-23-6-D	Si	SiN <sub>x</sub>	1137	1.98
Si-AlO <sub>x</sub> -35A-1	Si	AlO <sub>x</sub>	942	1.60
Si-AlO <sub>x</sub> -35B-3	Si	AlO <sub>x</sub>	1048	1.60
Si-AlO <sub>x</sub> -35C-4	Si	AlO <sub>x</sub>	1114	1.60
Si-AlO <sub>x</sub> -35C-5	Si	AlO <sub>x</sub>	998	1.64
Si-7-17-1-A	Si	SiN <sub>x</sub>	675	2.02
Si-7-17-1-B	Si	SiN <sub>x</sub>	675	2.02
Si-7-17-2-A	Si	SiO <sub>x</sub>	717	1.43
Si-7-17-2-B	Si	SiO <sub>x</sub>	717	1.43

Sample No.	Semiconductor	Insulator	Description	Insulator Thickness (Å)	Index of Refraction
Si-10-4-7-A	Si	1100 Å SiO <sub>x</sub>	Emitter Structures	-	-
Si-10-4-7-B	Si	1100 Å SiO <sub>x</sub>	Emitter Structures	-	-
Si-10-4-7-C	Si	1100 Å SiO <sub>x</sub>	Emitter Structures	-	-
Si-10-4-7-D	Si	1100 Å SiO <sub>x</sub>	Emitter Structures	-	-